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Ultra-Low Power PLL Design and Jitter Anaylsis

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ULTRA-LOW POWER PLL DESIGN AND JITTER ANALYSIS

BY

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Abstract

This thesis presents the design of ultra-low power Phase-Locked Loops (PLLs) intended for applications in the extended audio range. The PLL is well suited for battery operated systems, where small size and low power operation are crucially important. The two implementations presented are based on current controlled relaxation oscillator and a ring oscillator intended for the same frequency range. The frequency is controlled by a current that can vary from 2 to 74 nA. Using a reference frequency of ¼ of the typical watch crystal frequency, the user can select any integer multiple of 8.192 kHz up to the maximum of 122.88 kHz. The PLL circuits operate from a single 3 V supply and, depending on the actual output frequency, dissipate between 0.9-2 μW of power.

This work also investigates phase jitter in PLLs. Expressions for the period jitter caused by the current noise as well as the voltage noise present on the two rails (V_{dd} and V_{ref}) are derived. The theoretical results reveal that the current noise establishes a lower bound for jitter, which scales as the inverse of the square root of the selected current.

The numerical result has been put to test by two practical circuits, which consume between 300-660 nA of current and produce frequencies between 8.192–122.88 kHz. The measurements confirmed that the computed lower bound serves as a realistic estimate of the actual performance.

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Introduction

1.1 Thesis Organization

This thesis is organized as follows: Chapter 1 is the general introduction of the research work. Chapter 2 introduces basic concepts of PLL and PLL applications. Noise sources in PLL and clock jitter is described in Chapter 3. Chapter 4 presents the purpose and strategies of ultra low power design. Building blocks of PLLs and jitter analysis in this research work are discussed in Chapter 5 and 6 respectively. Chapter 7 illustrates the simulation and physical testing results and Chapter 8 concludes the thesis and proposes future work.

1.2 Background and motivation of this research

Phase-locked loops (PLLs) are ubiquitous circuit blocks in RF and mixed-signal integrated circuits. They are extensively utilized as on-chip clock generators to synthesize and de-skew a higher internal frequency from the external lower frequency. In data communications, serial links, and disk-drive read channels, PLLs are also employed as

clock recovery systems. In broadband optical communication networks, they are used as clock and data recovery (CDR) to generate the clock and decode the data from the received electrical signal. In wireless communication, they are utilized as frequency synthesizers to synthesize an accurate output frequency.

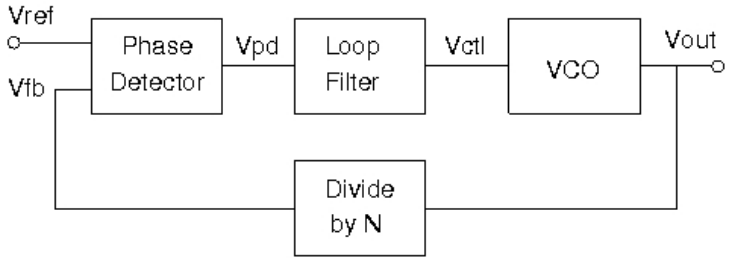

Figure 1.1. Block diagram of phase locked loop.

Figure 1.1 depicts the basic building blocks of a PLL: a phase detector (PD), a loop filter, a voltage controlled oscillator (VCO) and a (digital) frequency divider. The VCO and the loop filter are arguably the most critical blocks, since they decide about the frequency range and exert the strongest influence on settling behavior as well as frequency and phase stability.

Ultra-low power PLLs are highly desired for battery operated systems found in many wireless sensing applications or portable miniature

biomedical devices. Low power oscillators in PLLs are essential for battery-operated medical devices and remote sensing systems such as neural recording systems [1], [2], EEG/ECG and EMG monitors [3], wearable implantable medical sensors [4] and wireless sensing networks (WSN) nodes [5] in order to maximize the battery lifetime. Ring oscillators exhibit good performance for ultra low power operation when operated in the subthreshold region [13], but their accuracy and temperature drift are highly dependent on the bias-current stability. A low-power crystal oscillator using 90nm technology has been published in [14]. However, crystals suffer from bulky size and cost. Relaxation oscillators are a strong alternative which is usually applied in low power operation with competitive frequency accuracy. Relaxation oscillators do not require any external components and can be implemented inexpensively by standard CMOS technology. Thus, relaxation oscillators are well suited for ultra-low power biomedical data transmission and sensor applications.

Due to the ever increasing demand on accuracy and stability, low jitter oscillators and jitter analysis continue to be topics of great interest. In wireless communications [6], PLLs are utilized as frequency

synthesizers to synthesize an accurate frequency. In biomedical data transmission and sensor applications, PLLs provide accurate clock signal to high resolution analog to digital converters for weak bio-signal like neural, EEG/ECG, or EMG signals. In these applications, jitter, the aperiodic variations of the switching instances or zero crossings of a PLL output, is one of the most critical performance parameters [7]. Time jitter of a waveform synthesized by a PLL may lead to data errors and functionality failure. An interesting approach on characterization of the phase noise in oscillators due to supply and ground noise has been proposed [9]. This study brings up a mathematical method to investigate the timing jitter of single-ended and differential CMOS ring oscillators due to power and ground noise. However, this paper has treated the oscillator circuit in the presence of stochastic power supply and substrate noise as a deterministic system. Interesting work has been done using system transfer function analysis and stochastic models for the substrate and power supply noise, 1/f noise and thermal noise [8], [10]. Voltage control oscillator noise has been widely known as a dominate noise source in PLL circuits and some research also pay particular attention to low glitch charge pump and charge pump noise reduction [11]-[12].

1.3 Introduction of proposed circuit design and jitter analysis.

To achieve the intended ultra-low power dissipation, the VCOs in the proposed PLLs are carefully designed to minimize current consumption and all MOS devices in the analog section of the PLL are operated in the sub-threshold or weak inversion region. All digital units are based on static CMOS design techniques to optimize more power-efficiency. If we adopt the common 3V terminal standard of many button cell batteries, the total supply currents of the PLLs have to be limited to approximately 0.5 μA to meet the stated power requirement. The analog MOS devices must therefore be biased with currents not exceeding 100 nA. As stated above, this requires operating the transistors in the sub-threshold region, which renders them more susceptible to geometry mismatches and various sources of noise and other disturbances. It is therefore a particularly challenging task for circuit designers to maintain high quality performance.

With the exception of a purely digital PLL, jitter invariably depends on the integrity of the (local) rail voltages, including substrate. All these voltages are strongly affected by the physical layout. Consequently, these random variations cannot readily be quantified. We have

therefore concentrated our efforts on finding a realistic lower bound for jitter based on device noise. The lower bound of jitter is a prediction of noise in practical PLLs, thus it is very useful for jitter analysis. We assume that the core of the ultra-low power PLL is realized by a relaxation oscillator, which generates a sawtooth waveform. However, our analysis is also applicable to a ring oscillator implementation if one replaces the sawtooth by a triangular wave produced by the consecutive switching elements forming the ring.

Compact formulas for the total jitter of both relaxation and ring oscillators are provided and theoretical expressions for the current noise of a relaxation oscillator based PLL and a ring oscillator based PLL are presented. Since rail voltage fluctuations are strongly affected by injected noise, the more predictable current noise induced jitter is utilized as a lower bound.

To test the validity of the derived expression for lower bound of jitter, we have realized two slightly different versions of an ultra-low power low frequency PLLs in 0.5 μm CMOS technology. We also have fabricated both single-end and differential ring oscillator to investigate

the effect of supply and substrate noise on the performance of both structures. Two high speed differential ring oscillators with different number of stages are implemented to discuss the dependence of the jitter on power consumption and the number of stages.

1.4 Instruments and tools for design and testing

Design tools:

HSPICE for circuit simulation,

Magic for circuit Layout design.

ExpressPCB for PCB testing board design.

Testing instruments:

LeCroy WaveRunner Xi-A: 2 GHz, 4 Channel oscilloscope from ON Semiconductor Inc.

Tektronix MSO5204: 2 GHz, 4 Channel Oscilloscope from Tektronix Inc.

Matlab from Department of Electrical, Computer, and Biomedical Engineering at University of Rhode Island.

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Chapter 2

Introduction of PLL

2.1 PLL history

In the early 1930's, Edwin Howard Armstrong's superheterodyne receiver was very famous and he is widely regarded as one of the foremost contributors in the field of radio-electronics. In 1932, a scientist in France by the name of H.de Bellescise, wrote a subject on the findings of PLL (Phase-locked loop) "*La Réception Synchrone*" published in Onde Electrique, volume 11. His research was considered very carefully by a British scientist team as an alternative to Edwin Armstrong's superheterodyne receiver. They developed further Bellescise's theory and direct-conversion receiver as their invention was first consisted of a local oscillator, a mixer, and an audio amplifier. When the input signal and the local oscillator were mixed at the same phase and frequency, the output was an exact audio representation of the modulated carrier. Initial tests were encouraging, but the synchronous reception after a period of time became difficult due to the slight drift in frequency of the local oscillator. To counteract this

frequency drift, the frequency of the local oscillator was compared with the input by a phase detector so that a correction voltage would be generated and feed back to the local oscillator, thus keeping it on frequency. This technique had worked for electronic servo systems. This type of feedback circuit began the evolution of the Phase-Locked Loop. In analog television receivers since the 1930s to the 1940s, phase-locked-loop horizontal and vertical sweep circuits are locked to synchronization pulses in the broadcast signal.

Since that time, the phase-locked loop principle has been researched in academia. For instance, F.M Gardner and A. J. Viterbi published *Phase-Lock Techniques* and *Principles of Coherent Communications respectively* in 1966 *and* W.C. Lindsey wrote *Synchronization Systems in Communication and Control* in 1972. In the mean time, the electronic phase-locked loop principle has been extended to more industrial applications. For example, radio telemetry data from satellites used narrow-band, phase-locked loop receivers to recover low-level signals in the presence of noise. When Signetics (the first electronics manufacturer of integrated circuits) introduced a line of monolithic integrated circuits such as the NE565 that were complete

phase-locked loop systems on a chip in 1969, applications for the technique multiplied. A few years later RCA introduced the “CD4046” CMOS Micropower Phase-Locked Loop, which became a popular integrated circuit.

Nowadays, PLLs are very widely used to demodulate frequency-modulated signals, such as AM and FM demodulators and FSK decoders. They can be also used for synchronization purposes such as in space communications for coherent demodulation and threshold extension, bit synchronization, and symbol synchronization. Other applications are as lock-in amplifier and clock multipliers in microprocessors.

2.2 Basic block diagram of PLLs

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input "reference" signal. As depicted in Figure 2.1- the basic building blocks of a PLL are a phase detector (PD), a loop filter, a voltage controlled oscillator (VCO) and a (digital) frequency divider.

This circuit compares the phase of the input signal (V_{ref})with the phase of the signal derived from its output oscillator (V_{fb}) and adjusts the frequency of its oscillator to keep the phases matched. The signal from the phase detector is used to control the oscillator in a feedback loop.

The VCO and the loop filter are arguably the most critical blocks, since they decide about the frequency range and exert the strongest influence on settling behavior as well as frequency and phase stability.

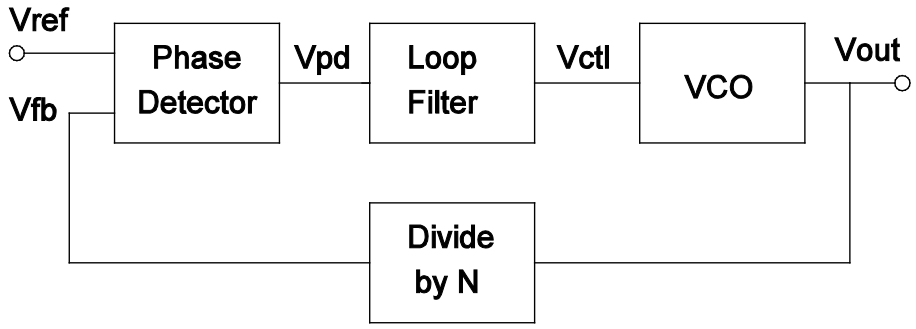

Figure 2.1 Basic PLL block diagram.

The loop filter is typically a simple first or second order passive RC circuit. In cases where it is necessary to reduce clock misalignment, active filters can be used as well. While they can yield more effective filter characteristics, they add significantly more complexity to the control of the settling behavior and the locking characteristics. If the

PLL output frequency is expected to be an integer multiple of the reference, the feedback path has to incorporate a digital frequency divider or modulo counter. If the frequency division is programmable, the PLL can serve as a frequency synthesizer.

2.3 Classifications of PLLs and Oscillators

2.3.1 Classified by PLLs' characters

There are several variations of PLLs. Some terms that are used are analog phase-locked loop (APLL) also referred to as a linear phase-locked loop (LPLL), digital phase-locked loop (DPLL), all digital phase-locked loop (ADPLL), and software phase-locked loop (SPLL).

Analog PLL (APLL) and digital PLL (DPLL)

The main difference between a analog PLL and a digital PLL is the phase detector. Analog PLLs use multipliers to find the difference between two analog signal, while digital PLLs use exclusive-OR (XOR) logic gates, flip-flops or tri-state phase frequency detectors, to find delays between two analog signals.

The analog phase detector needs to compute the phase difference of its two input signals. Let α be the phase of the first input and β be the phase of the second. The actual input signals to the phase detector, however, are not α and β, but rather sinusoids such as sin(ωt+α) and cos(ωt+β). In general, computing the phase difference would involve computing the arcsine and arccosine of each normalized input and doing a subtraction. Such an analog calculation is difficult. Fortunately, the calculation can be simplified by using some approximations.

Assume that the phase differences will be small (much less than 1 radian, for example). The small-angle approximation for the sine function and the sine angle addition formula yield:

$$\alpha - \beta \approx \sin(\alpha - \beta) = \sin\alpha\cos\beta - \sin\beta\cos\alpha \; . \qquad (2.1)$$

The expression suggests a quadrature phase detector can be made by summing the outputs of two multipliers. The quadrature signals may be formed with phase shift networks. Two common implementations for multipliers are the double balanced diode mixer (diode ring) and the four-quadrant multiplier (Gilbert cell).

Instead of using two multipliers, a more common phase detector uses a single multiplier and a different trigonometric identity:

$$\sin\alpha\cos\beta = \frac{\sin(\alpha - \beta)}{2} + \frac{\sin(\alpha + \beta)}{2} \approx \frac{\alpha - \beta}{2} + \frac{\sin(\alpha + \beta)}{2} \qquad (2.2)$$

The first term provides the desired phase difference. The second term is a sinusoid at twice the reference frequency, so it can be filtered out.

The digital phase detector is based on logic gates, it can quickly force the voltage controlled oscillator to synchronize with an input signal, even when the frequency of the input signal differs substantially from the initial frequency of the voltage controlled oscillator. Such a phase frequency detector has the advantage of producing an output even when the two signals are compared not only in phase but also in frequency. A digital phase detector also has better accuracy in case there are only small phase differences between the two input signals.

All digital PLL (ADPLL)

Integrating an analog PLL in a digital noisy environment such as in high speed microprocessors is difficult. In addition, the analog PLL is sensitive to process variations. So all digital PLLs have also been investigated and implemented. All the PLL components (phase

detector, loop filter and oscillators) are digital. Figure 2.2 shows the basic diagram of an all digital PLL system. Digitally controlled oscillator is the replacement of the analog voltage controlled oscillator and analog loop filter is replaced by the time to digital converter.

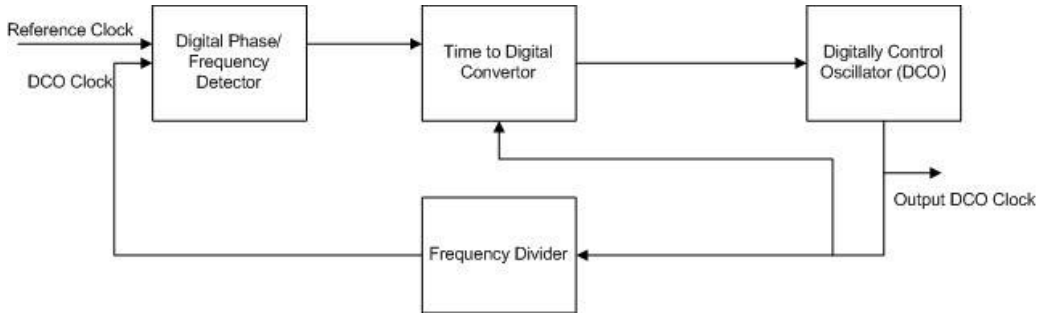

Figure 2.2. All digital PLL block diagram.

The analog loop filter is based on charging and discharging a capacitor to generate certain control voltages in response to information provided by the phase detector. The time to digital converter consists of a down counter, up counter, and carry ripple adder as illustrated in Figure 2.3. The phase detector (previous stage) controls the up counter and down counter by up and down enable signals. The up counter and down counter values are inputs to the carry ripple adder and the output forms the control word for the digitally controlled oscillator (DCO). The converter should be active only if there is a phase and/or frequency mismatch. Clock gating has been performed to disable the

time to digital converter when both the reference clock and divided DCO clock are locked.

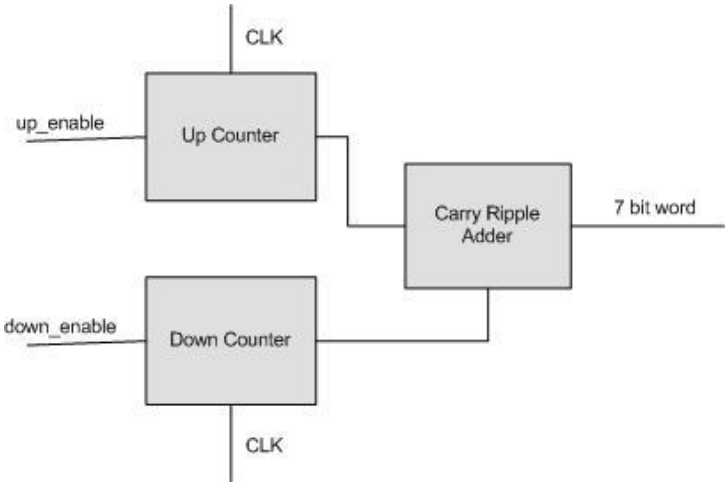

Figure 2.3. Time to Digital converter.

There is one extra block right after the time to digital converter - the thermometric decoder- which is a specific decoder that generates the digital word C (an N-bit vector) that controls the digitally controlled oscillator (DCO). A typical digital controlled oscillator is shown in Figure 2.4.

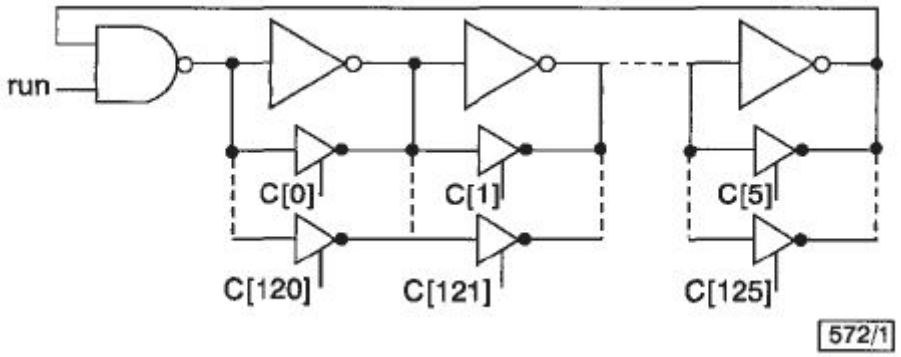

Figure 2.4. Digitally controlled oscillator.

The oscillator is a multiple-stage ring oscillator with one inverter replaced by a NAND-gate for shutting down the ring oscillator during stand-by mode. The RUN signal on one of the NAND inputs controls the oscillator in active or stand-by mode. To change the frequency of the ring oscillator, a set of inverting tri-state gates, as shown in Figure 2.4, connected in parallel with each inverter, are used to change the current of each inverter. The tri-state gates are controlled by a digital word C (N-bit vector).

Software PLL (SPLL)

All of the components are implemented by software rather than hardware. The signal processing performed by a PLL can be carried out by a hardware platform such as digital signal processor (DSP) or a

microcontroller. This type of PLL is usually called software PLL and the function of the PLL is realized by software. The processing is achieved by mathematical algorithms running on a microprocessor. The implementation is normally achieved by a field-programmable gate array (FPGA). Software PLLs have many advantages compared to hardware-based PLLs, such as their immunity to noise and high accuracy. Furthermore, the reconfiguration capability of programming enables developing a large number of different algorithms. For example, an SPLL can be programmed as an APLL, a DPLL, or an ADPLL. Of course, the SPLL can compete with a hardware solution only if the algorithms are fast enough to run on the hardware platforms.

2.3.2 PLL Internal Oscillator Classification

Oscillator is the most critical cell in a PLL, so we introduce different types of oscillators that can be used in a PLL design. If we classify oscillators by the number of energy storage elements, LC and crystal oscillators are characterized by two energy storage elements. Relaxation oscillators are considered to have one energy storage element. Ring Oscillators are characterized by more than two energy storage elements, since the ring is composed of multiple stages.

Crystal and LC oscillators are operating in resonance. Resonant circuit-based VCO's are known to have excellent jitter performance [1], [2]. Unfortunately, the requirement of an off-chip tank or crystal defeats the purpose of integrating the PLL function.

VCOs based on RLC oscillators typically have a high quality factor Q, that can substantially reduces their sensitivity to noise sources, but VCOs based on RC oscillators, such as relaxation or ring oscillators, have a low-Q and thus are relatively sensitive to noise. Furthermore, the limited frequency range and the larger chip area requirement of LC oscillators can make an LC VCO implementation impractical. Thus, how to choose an oscillator for PLL is based on application requirements.

Ring Oscillator

The ring oscillator is designed with a chain of delay stages. The output frequency of a ring oscillator depends on the delay of each stage and the number of stages. The conceptual diagram is shown in Figure 2.5.

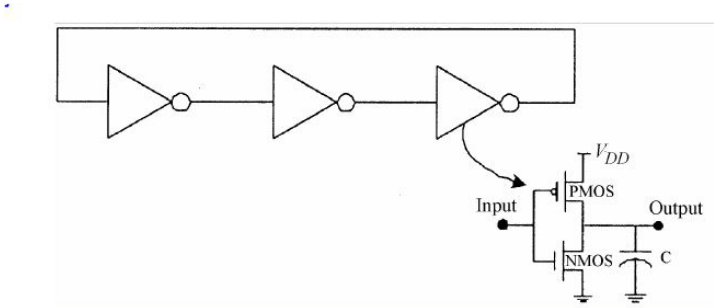

Figure 2.5. Conceptual diagram of ring oscillator.

In Figure 2.5, the delay cells are single-ended inverters. Fully differential inverters are normally used in practical designs because they have a much better common mode rejection ratio (CMRR) and stronger supply and substrate noise immunity. The ring oscillator has created great interest because of its numerous useful characteristics:

1. It can be easily designed with state of art integrated circuit technology. Due to its ease of integration, ring oscillators are increasingly being used as voltage controlled oscillators in jitter sensitive applications.

2. It occupies small area, but ring-VCOs are sensitive to supply noise. If the noise and supply-sensitivity issues of ring-VCOs are addressed, these VCOs would be ideally suited for applications

such as serial links. Some design techniques for improving jitter exist and empirical results show promise of excellent jitter performance [3].

3. It can oscillate to achieve a wide tuning range under low voltages, so it is a good choice for high frequency applications demanding low power and low frequency applications with ultra-low power and low jitter. For example, ring oscillators exhibit excellent characteristics for ultralow power operation when operated in the subthreshold region [4], but their accuracy and temperature drift are determined by the bias-current stability [5]

4. It can provide multiphase outputs because of their basic structure. These outputs can be logically combined to realize multiphase clock signals, which are well suited for a large number of applications in communication systems and microprocessor timing manage systems.

5. Other applications including disk drive clock recovery [6] [7], clock frequency multiplication [8] [9] and oversampling analog to digital

converters (ADCs) would benefit from the cost and size advantages of fully integrated and low jitter ring oscillator.

Relaxation Oscillator

A relaxation oscillator has one energy storage element with additional circuitry that senses the element state and converter this periodic excitation to a periodic output signal [10]. As shown in Figure 2.6, the energy storage element is C_R. The capacitor generates a sawtooth wave by integrating a constant current. Normally a comparator normally is used to reset the voltage across the capacitor by comparing it to $V_{ref.}$

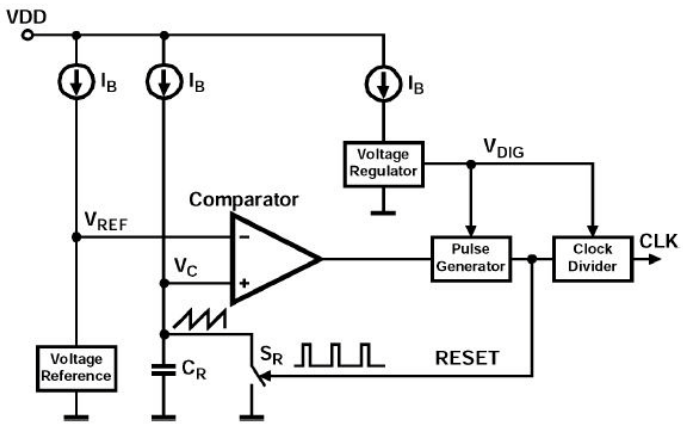

Figure 2.6. Conceptual diagram of relaxation oscillator.

Relaxation oscillators are usually employed for low-power operation with a relatively good accuracy. They are often used in micro controller or biomedical ASICs (application-specific integrated circuit) where the frequency is quite low. In addition, fully integrated clock

recovery PLL's have been published using relaxation oscillators [11], [12]-[14].

For low frequency and relatively low frequency precision applications, relaxation oscillators are preferred against crystal oscillators and LC oscillators because of several reasons as listed below:

1. Relaxation oscillators do not require any external components and can readily be implemented in CMOS technology.
2. Relaxation oscillators draw less current than crystal oscillators at the cost of larger clock jitter, so they are a good solution for ultra-low power design in biomedical applications.
3. Relaxation oscillators are not necessary to use extra components, so they have smaller size than LC oscillators.

For those applications that have very strict and extremely low jitter request, harmonic oscillators (crystal oscillators and LC oscillators) are preferred. Relaxation oscillators yield more jitter than harmonic oscillators. The absolute frequency accuracy of relaxation oscillators is affected by the accuracy of on-chip capacitors and resistors that determine the frequency of the oscillator. Jitter analysis for this type of oscillator has been carried out in the time domain [10], [15], [16].

Crystal Oscillator (XCOs)

A quartz crystal is a resonant element. A crystal oscillator is operating in resonance. Quartz crystals are modeled electrically as a series LC branch in parallel with a shunt capacitance C_0 as shown in Figure 2.7. *T*he series LC branch, often called the motional arm, models the piezoelectric coupling to the mechanical quartz resonator. C_1 is the motional capacitance, R_1 is an equivalent series resistance, L_1 is called motional inductance. Its value can be determined by C_1 and the operating frequency. C_0 is the shunt capacitance. The shunt capacitance represents the physical capacitance formed by both the parallel plate capacitance of the electrode metallization and the stray package capacitance.

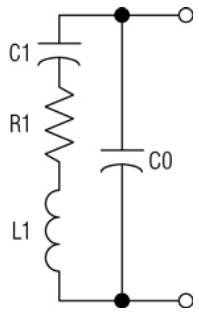

Figure 2.7. Quartz crystal model.

Crystal oscillators are superior frequency generators with excellent stability with respect to variations of supply voltage, temperature, and

process. The feasibility of low-power operation in nano-scale technology has been reported in [17]. However, crystals are bulky devices and lead to excessive system cost.

LC Oscillator

LC Oscillators are commonly used in radio-frequency circuits because of their good phase noise characteristics. LC oscillators [18] can provide good accuracy and phase noise performances comparable to XCOs; however, their power consumption is high due to the limited Q of the integrated inductors.

In an LC oscillator, energy is moved between two energy storage elements (capacitor and inductor) and stored in form of a magnetic field in the inductor and an electric field in the capacitor. Figure 2.8 is an ideal model illustrating the principle of LC oscillator. When the current flowing in the LC tank approaches the maximum, there is no voltage across the tank. When the voltage across the tank is maximum, all energy is transferred into the electric field. In an ideal LC oscillator, energy can be converted back and forth between capacitor and inductor. The LC oscillator is oscillating without energy loss.

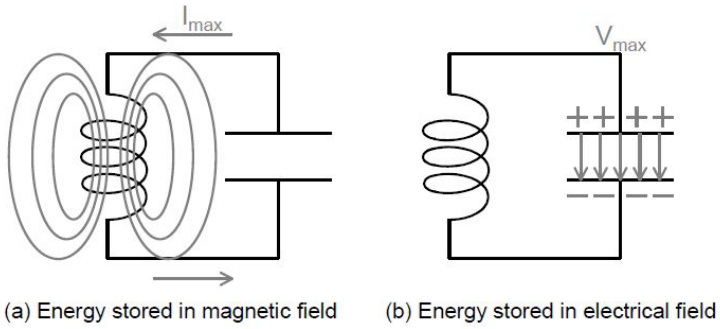

Figure 2.8. Operation of LC oscillator.

In practical application, energy loss is addressed by the non-idealities of the components of the LC oscillator. A practical model is depicted in Figure 2.9.

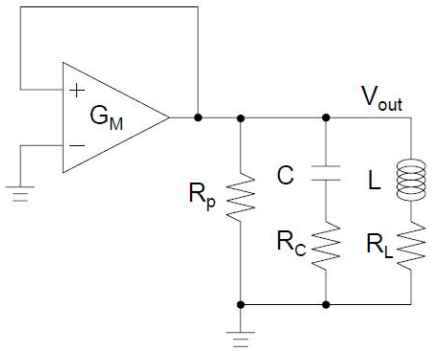

Figure 2.9. A practical model of LC oscillator.

R_c and R_L are parasitic resistances from the non-idealities associated with the capacitor and inductor, respectively. The output resistance of the transconductance and the parallel parasitic resistance of the LC tank are combined into R_p. The purpose of adding a transconductance G_m connected in positive feedback is to exhibit a negative resistance of

$-1/G_m$ and compensate for the energy losses caused by the parasitic resistance and thus guarantee the LC tank to oscillate.

A fully differential LC oscillator as displayed in Figure 2.10 is widely used because it reduces common mode noise like power supply and substrate noise. A similar topology is used in ring oscillators for the same purpose. A fully differential LC oscillator naturally yields low jitter performance as mentioned previously. There are three factors contributing to this characteristic. Firstly, the oscillator frequency of the LC oscillator is determined by passive components. They provide less noise and less instability than active components. Secondly, the low gain minimizes PLL sensitivities to supply and substrate noise. Low gain also reduces the impact from charge-pump noise. Thirdly, the differential topology further boosts the LC oscillator's noise immunity. However, LC oscillators usually occupy a large die area and feature a narrow tuning range. These drawbacks limit their use to narrow band and low jitter, low phase noise applications.

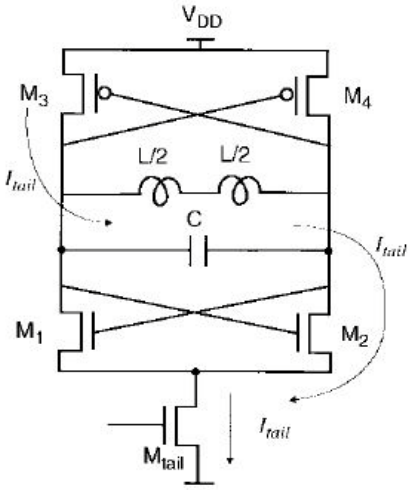

Figure 2.10. Differential LC oscillator.

2.4 PLL Applications

PLLs are versatile building blocks used in many communication systems and integrated circuits, where they serve as clock recovery, frequency deskewing, frequency synthesis, spread spectrum, clock jitter reduction units, etc. In high speed systems, the trend towards low power and small area increases the demand for low jitter, low phase noise, high integration and flexibility of fabrication. In low speed systems, ultra low power, extreme clock accuracy and good noise immunity are mandatory. Therefore, PLLs are the most popular fundamental clock generating circuits. PLL circuits can be readily adapted to high bandwidth, mid-bandwidth or low bandwidth.

Furthermore, they are small units with great topological flexibility. For instance, analog PLLs, digital PLLs, all digital PLLs and software PLLs are developed for different applications, ring oscillator PLLs serve in typically used for high frequency applications and relaxation oscillator PLLs for low jitter designs.

2.4.1 Clock recovery

In certain data communication applications and high speed magnetic recording data system (disk drive control), clock recovery is challenging and must be performed with strict requirements on phase matching, sensitivity to decoding errors, phase jitter and programming capability. Some signals are sent out without accompanying a clock. The receiver generates a clock from a reference frequency and then synchronizes the transitions to the data stream by using a PLL, which extracts a clock from the incoming signal. This mechanism is referred to as clock recovery. It is typically combined with some decoding technologies. For example, two common encoding methods are Return to Zero (RZ) and Non-Return to Zero (NRZ). Another broad use of PLLs is in storage systems (hard disks). Disk drives encode the cross-track position in a variety of ways, but they all require some type of PLL to synchronize the reading of the position signal with the

rotation of the disk. In general, a clock must be recovered at the beginning of each sector. Currently, encoding schemes are classified into two groups. The most common encoding is called amplitude encoding. The alternative is phase encoding of position error. In this case the phase difference between the reference mark and the position mark provides a measure of the cross track position. Overall, most high-speed clock recovery circuits make use of an analog PLL.

2.4.2 Deskewing

In communication system, clocks are used to sample the data. If the received clock for data sampling has a delay with respect to the received data window, the sent data will not be received correctly. This phenomenon is called clock skewing. One way of eliminating this delay is to integrate a deskew PLL in the receiver circuitry. In the microprocessor field, the clock delay occurs between external and internal clock (clock skew) caused by the propagation delay of the on-chip clock driver as indicated in Figure 2.11.

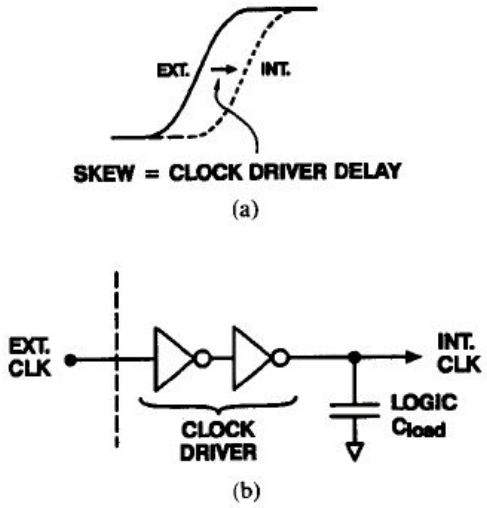

Figure 2.11. Clock skew definition.

As clock frequency increases to 50MHz and higher, the clock skewing is caused by large setup and hold times for input/output signals. The delay will limit the frequency of the microprocessors. As the microprocessor increases in size to 1 million transistors and beyond, the capacitive loading of the logic circuits on the clock driver is growing to values of several nanofarads. Therefore, the delay through the clock driver can be several nano seconds. In order to implement much faster and more complex integrated microprocessors, on-chip PLLs are used to eliminate the clock skew caused by the clock driver.

2.4.3 Frequency synthesis

The frequency synthesizer is one of the most critical blocks in wireless transceiver as shown in Figure 2.12. Large bandwidth, high frequency accuracy, and low phase noise is highly desirable when the synthesizer is used as a frequency modulator and demodulator. Thus, PLLs are widely used in this area.

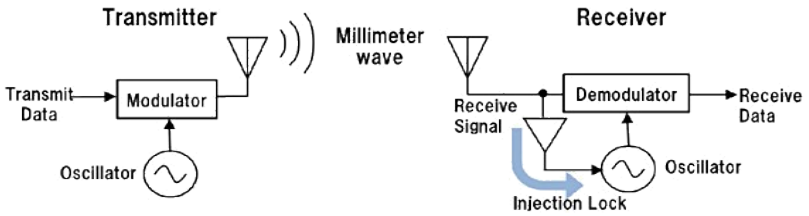

Figure 2.12. Transceiver system diagram.

Its performance directly affects the transceiver's noise figure, image rejection and spurious emission. The voltage controlled oscillator is very sensitive to interference from power supply noise, substrate noise, temperature and process variations, etc., especially in systems that transmit a high power and high frequency signal.

In current generation computer systems, PLL frequency synthesizers have been used to provide low jitter, low phase noise signals as a source clock generator to replace various crystals or resonators.

Besides the use for high frequency communication and computer applications, PLL can also be used as low frequency synthesizers for biomedical systems and wireless sensor networks (WSN).

The dominant energy of wireless sensor networks (WSN) consumed in each node of a WSN is spent in idle listening to the channel while waiting for data packets [2]. This task requires a synchronization algorithm to ensure that all nodes observe simultaneous sleep and wake-up times and, consequently, each node must be equipped with a time reference to enable such synchronization. A high accuracy clock reference is required by the receiver to accurately predict the timeslot used by the transmitter. Crystal-controlled oscillators (XCOs) can generate a fine frequency solution, but they are bulky external components. Furthermore, they are costly and very inconvenient in wireless applications. In order to realize miniature WSN nodes and lower the cost, accuracy must be traded for the sake of integration. So, ring oscillators or relaxation oscillators are better solutions for PLLs in WSN applications.

Biomedical systems increasingly require minimum power circuits to

provide for a longer battery lifetime. Low power building blocks are essential for battery-operated portable medical devices such as ECG/EKG monitors, heart rate monitors, blood glucose meters, or nerve signals analyzer in order to reduce the system cost in spite of increased energy demand. Thus, low jitter low-power PLLs are well suited for these applications. For example, the ECG/EKG signal range is 100 μV to 10 mV, therefore, they need a high resolution, high noise rejection system to extract and convert biologic signal from noisy background to digital signal. Normally, a preamplifier and an analog to digital converter (ADC) are essential units in the system. Therefore, a small PLL circuit will be required to provide a low jitter, high precision clock signal for the ADC. For instance, to achieve 16 bit 2 kHz ADC over a 1 kHz band, the clock jitter should be less than 2.4 ns.

2.4.4 Spread spectrum

All electronic systems emit unwanted radio frequency energy. The emitted noise generally appears at the operating frequency of the device and at a few harmonics. A spread spectrum PLL is a reliable building block to reduce the spectral amplitude of the EMI (Electromagnetic interference) components over a substantial

bandwidth and mitigate interference by spreading the energy over a large portion of the spectrum. By spreading the bandwidth, the amplitude of the signal is decreased with respect to its fundamental and harmonics. As a result of reducing the peak amplitudes, the peak radiated electromagnetic emission level is dramatically lower when compared to a typical narrow band signal without spreading the spectrum.

Several spread spectrum methods have been used over the past 10 years as is evident from the literature. Some researchers changed the operating frequency up and down by 1% to spread the spectrum by 1%. A device running at hundreds of MHz can spread its interference evenly over a few MHz. The smooth frequency transition PLL can also be used to spread the clock signal spectrum. This cuts down the spectrum energy of the fundamental and harmonic frequencies without timing tolerance degradation of the peak frequency. A clock signal can also be modulated to the spread spectrum of the fundamental frequency by injecting a modulating signal into the feedback path of the PLL. A block diagram of a spread spectrum PLL with signal modulating is shown in Figure 2.13. The output clock signal spectrum with and

without spreaded spectrum is shown in Figure 2.14.

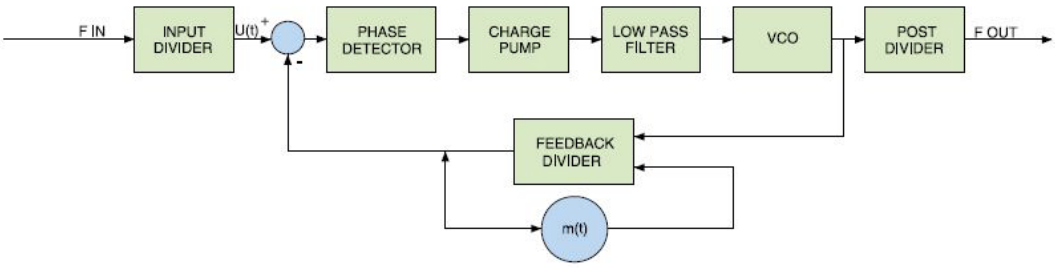

Figure 2.13. Block diagram of spread spectrum PLL.

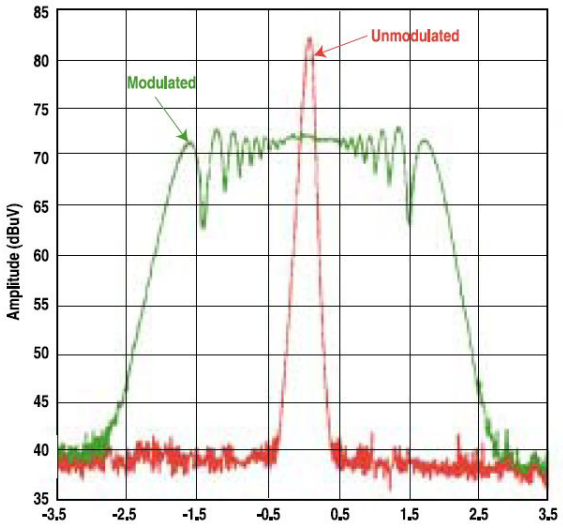

Figure 2.14. Modulated and unmodulated clock spectrum.

2.4.5 Clock distribution

Clock distribution is one of the most important areas in the design of high performance VLSI chips. Difficulties of clock distribution in nanometer technologies in terms of reliability and power efficiency are underlined in numerous recent studies [1][2]. Poor clock distribution

can result in excessive clock skews on the chip, reducing the maximum operating frequency. In modern technologies, traditional clock distribution approaches (such as clock tree, clock grid, etc) suffer from uncertainty of increased propagation delays and supply noise.

To get around these difficulties, several recent architectures of global clock generation have in common a distributed generation of the clock signal. This is generally achieved using an array of PLLs, each PLL being placed in the center of the local synchronous area. The PLL strives to minimize the skew between the external and internal clocks through its phase alignment performance. It is important to design a low skew clock distribution network to maximize the high performance microprocessor's operating frequency. A simplified clock distribution system with a PLL is indicated in Figure 2.15.

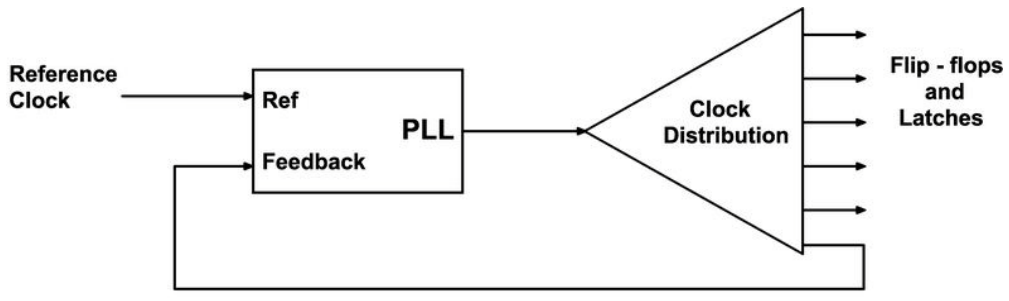

Figure 2.15. Simplified clock distribution with PLL.

2.4.6 Jitter and noise reduction

In high frequency interfaces, PLLs can be used to filter high frequency noise and produce a low jitter sampling clock. Jitter attenuation is determined by the frequency response of the PLL loop filter. The filter is a low-pass filter with a very low cutoff frequency. Jitter at frequencies above this cutoff frequency will be filtered and below this cutoff frequency will be left. The input reference clock and a divided version of the output clock signal are input signals of the phase frequency detector. The output of phase frequency detector including noise from the input reference clock goes through the loop filter. Therefore, the loop filter partially removes noise components from the input reference clock. Hence, the PLL output clock is a cleaned up signal that can be used for the rest of the circuit. However, we have to make sure that the filtered out noise is much less then the noise generated from the PLL itself.

PLLs are devices used to align the phase of a generated clock signal to an input reference clock signal. They often provide multiplication and division of the reference clock frequency and, as a byproduct of the usage of a low-pass filter, they can remove some level of jitter. Lower

cutoff frequencies of the loop filter can reduce more high frequency noise, but higher cutoff frequencies are required to achieve reasonable lock times. Therefore, a PLL is a good compromise considering all the performance factors.

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Chapter 3

Introduction of Noise in PLL and clock jitter

PLLs are widely used in high performance mixed signal systems. PLLs multiply low frequency reference clocks to produce low-jitter, higher frequency clocks for subsequent circuits. For many applications, clock jitter and power dissipation are two important design criteria. In this chapter, we present an introduction of PLL noise and clock jitter. Low power PLL design will be discussed and addressed in the following chapter.

3.1 Noise in PLL

A PLL is always operating in a noisy environment. That includes device electronic noise as well as supply and substrate noise. Thermal noise, shot noise and flicker noise in MOSFETs are components of electronic noise caused by internal electrical characteristics. Power-supply and substrate noise results from switching activities in integrated mixed signal systems. They perturb the most sensitive

blocks in a PLL. In particular, any noise injected into the voltage controlled oscillator (VCO) elements and the charge-pump forms a dominant source of phase noise of a PLL.

Thermal noise is charge fluctuation caused by the random Brownian motion of electrons in a resistive medium. It is broadband white noise, whose power increases with temperature and decreases with resistance. The spectral density of the thermal noise on the current across a resistor with resistance R is given by

$$I_n^2 = 4k\ T/\ R \tag{3.1}$$

A fifty ohm resistor has about $1nV/\sqrt{Hz}$ of thermal noise at T=300k.The thermal noise term of a MOSFET is straightforward. In the triode region, the thermal noise current density due to the channel resistance is simply

$$I_d^2 = (4kT / r_{ds}) \tag{3.2}$$

where r_{ds} is the channel resistance. However, when the transistor operates in the active region, the channel cannot be considered homogeneous, and thus, the total noise is found by integrating over small portions of the channel. Such an integration results in the

following noise current density

$$I_d^2 = 4kT(\frac{2}{3})\mathrm{g_m} \tag{3.3}$$

where g_m is the transconductance. Noise analysis implies adding this noise source between the transistor drain and source. However, one should be aware that this simplified model (3.3) assumes zero gate current. Although this assumption is valid at low and moderate frequencies, an appreciable amount of current will flow through the gate-source capacitance, C_{gs}, at higher frequencies. Finally it should be noted that no gate leakage noise terms have been included in this noise model since, in modern processes, the gate leakage is so small that its noise contribution is rarely significant.

Shot noise is caused by the fact that current flowing across a junction is not smooth, but rather consists of individual electrons arriving at random times. This non-uniform flow gives rise to broadband white noise that increase with the average current. The spectral current density of the shot noise associated with a junction current I is given by

$$I_n^2 = 2 \cdot \mathrm{q} \cdot \mathrm{I} \tag{3.4}$$

where q is the electronic charge (1.6×10^{-19} C).

Shot noise is typically the dominant noise in diodes and can be modeled by a current source in parallel with the small signal resistance of the diode. If the MOS transistor is operating in the subthreshold region, the accuracy of the square-law equation for saturation is poor. The transistor is more accurately modeled by an exponential relationship between its control voltage and current, somewhat similar to a bipolar transistor. Thus, MOSFETs in subthreshold exhibit shot noise instead of thermal noise due to the current flowing in the channel. This noise source has the standard form.

$$I_d^2 = 2 \cdot \mathrm{q} \cdot \mathrm{I_d} \tag{3.5}$$

Flicker noise is low frequency noise in silicon MOSFET. Because MOSFETs have large flicker noise components, it sets a lower limit to the level of signal that can be processed by VLSI devices and circuits. Much effort has been spent in understanding and reducing noise for better performance in VLSI circuits. In the past five decades, a considerable number of papers have been published dealing with flicker noise in MOSFETs [1]-[9].

Flicker noise was first observed in vacuum tubes over seventy-five years ago [10]. It gets its name from the anomalous “flicker” that was

seen in the plate current. It is commonly known as 1/f noise since the noise spectral density is inversely proportional to frequency. The flicker noise spectrum varies as $1/f^{\alpha}$, where the exponent α is close to unity (α=1±0.2). Fluctuations with a 1/f power law have been observed in practically all electronic materials and devices, including homogenous semiconductors, junction devices, metal films, liquid metals, and electrolytic solutions. In addition, it has been observed in mechanical, biological and geological systems. No entirely satisfactory physical explanation has been developed, and in fact, available evidence seems to suggest that the origins of flicker noise in different devices may be quite different [11]. Two competing models have appeared in the literature to explain flicker noise: the McWhorter number fluctuation theory and the Hooge mobility fluctuation theory.

The spectral density $V^2_n(f)$, of 1/f noise is approximated by

$$V_n^2(f) = \frac{K_v^2}{f} \tag{3.6}$$

where K_v is a constant. In terms of root spectral density, 1/f noise is given by

$$V_n(f) = \frac{K_v}{\sqrt{f}} \tag{3.7}$$

V_n is inversely proportional to $\sqrt{f}$. An example of a signal having both 1/f and white noise is shown in Figure 3.1. Note that 1/f noise falls off at a rate of -10 dB/decade since it is inversely proportional to $\sqrt{f}$. The intersection of the 1/f and white noise curves is often referred to as the 1/f noise corner .

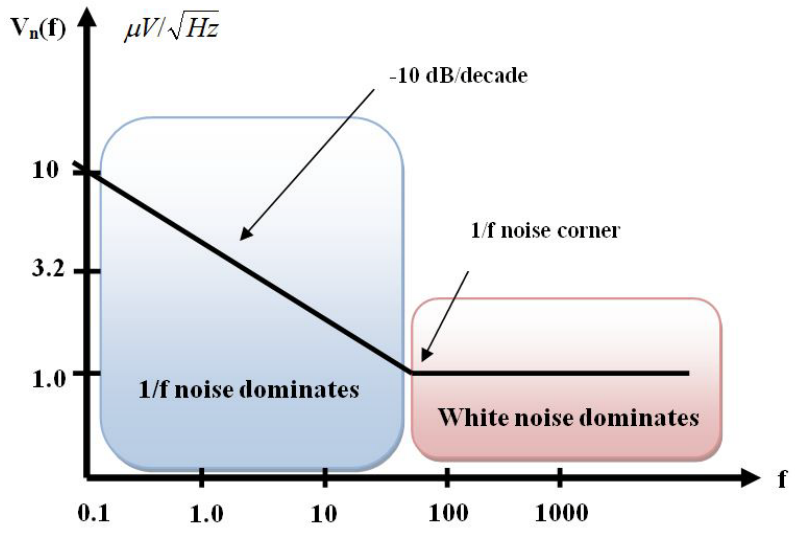

Figure 3.1. A noise signal that has both 1/f and white noise.

If we only consider device electronic noise in a PLL circuit, flicker noise is very important as long as the PLL operates below several kHz. Since thermal noise is always present and has an even strength over the whole bandwidth, the noise spectral density of a low speed PLL will have a shape similar to that illustrated in Figure 3.1. On the other hand, if a PLL's output frequency is in the MHz or GHz range, flicker noise

is significantly compressed and typically negligible compare to thermal noise, making thermal noise the dominant electronic device noise.

Supply and substrate noise are other key factors that to influence the performance of PLLs. Recall that power supply noise and substrate noise are caused by switching. Because of this, integrating an analog circuit required to generate precision timing on a compact die such as a microprocessor, which has a large amount of digital switching noise is difficult. The more we push speed, the more we have to cope with supply and substrate noise. Some researchers point out that device noise can be neglected since it pales compared to supply and substrate noise in high speed systems [12].

Supply and substrate noise are inherently stochastic. They depend on the physical operating conditions such as the cross talk between analog and digital signals. Recently, interesting approaches on the characterization of supply and substrate noise have been proposed, which utilize deterministic noise model to simplify the analysis. The noise behavior is modeled as a small sinusoidal perturbation [13], [14] as revealed in (3.8). In this work, we modeled random noise as a finite

sum of small sinusoids, which, we believe, has a broader applicability and practical significance.

$$\Delta V_m(\mathrm{t}) = \mathrm{V_m} \cos \omega_m t \tag{3.8}$$

By using the McWhorter number fluctuation theory, the calculated 1/f noise for the low frequency PLLs (10-150 kHz) turns out to be negligible compared to other noise sources. Consequently, thermal noise, shot noise and power supply or substrate noise are the noise components used to calculate the noise power density in this PLL research. The contribution of device electronic noise to phase jitter is not negligible in low power and low frequency applications. However, as exemplified by measured results reported in the literature, the contribution of device electronic noise to the PLL jitter performance is typically much less than that due to supply and substrate noise in high speed systems.

3.2 Charge pump and VCO non-idealities due to noise

Noise impacts the most sensitive blocks in a PLL, therefore, the two most critical jitter sources are the charge-pump and voltage-controlled oscillator (VCO)

3.2.1 Noise in charge pump

Non-idealities such as charge sharing, clock feedthrough, and current and timing mismatches are manifestations of noise. We discuss the impact of non-idealities to the charge pump circuit and describe several measures to reduce them.

Charge sharing

Figure 3.2 presents a charge pump as described in [15]. The UP (up) and DN (down) signals switch current sources I_{up} and I_{dn} onto node $V_{control}$, thus delivering a charge to move $V_{control}$ up and down. I_{up} and I_{down} need to be equal.

The charge sharing effect occurs between the common source nodes N1 and N2 of the PMOS and NMOS differential pairs and the output $V_{control}$ of the charge pump circuit. Any charge sharing from the parasitic capacitance on N1 and N2 can cause mismatch the UP and DOWN current sources.A unity-gain amplifier as shown in Figure 3.2, can be used to bias N1 and N2 when they are not switched to $V_{control}$. This suppresses the charge sharing problem. Another way to prevent the charge sharing problem is to employ a large capacitor on the

common source nodes (N1 and N2) [16] [17].

Clock feedthrough and charge injection

Charge injection and clock feedthrough are fundamental problems in analog ICs. Circuits such as analog-to-digital converters (ADC), digital-to-analog converters (DAC) and charge pumps are limited in performance due to the effects of charge injection and clock feedthrough. The charge injection occurs when the transistor switch is turned off as presented in Figure 3.3, dispersing the charge in the inversion channel, either into the substrate or the sampling capacitor at the MOSFET drain or source. This mechanism produces an error voltage on the sampling capacitor. The sampling capacitor on the source terminal experiences an error in the sampled voltage due to the incoming channel charge. The overlap gate-source capacitor also contributes to the total error voltage. This effect is called clock feedthrough. Charge injection and clock feedthrough problems are alleviated by placing the charge pump switches close to supply and ground rails [20]. Charge cancellation is another approach to reduce charge injection. Dummy transistors are used to provide the glitch pulses with polarity opposite to those erroneous glitches generated by

charge injection.

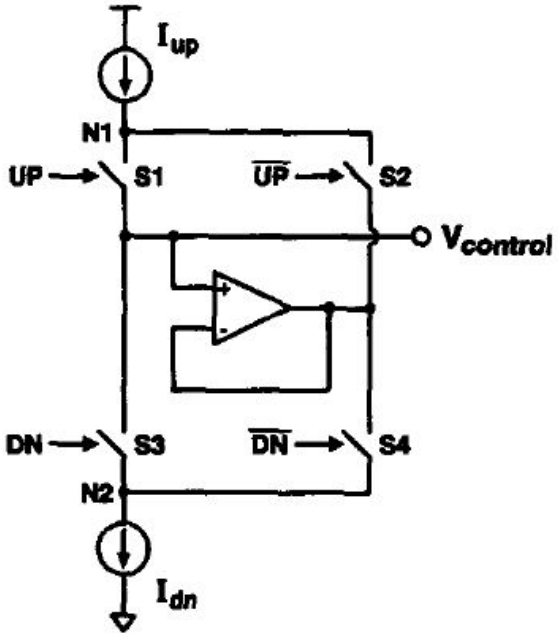

Figure 3.2. Charge pump.

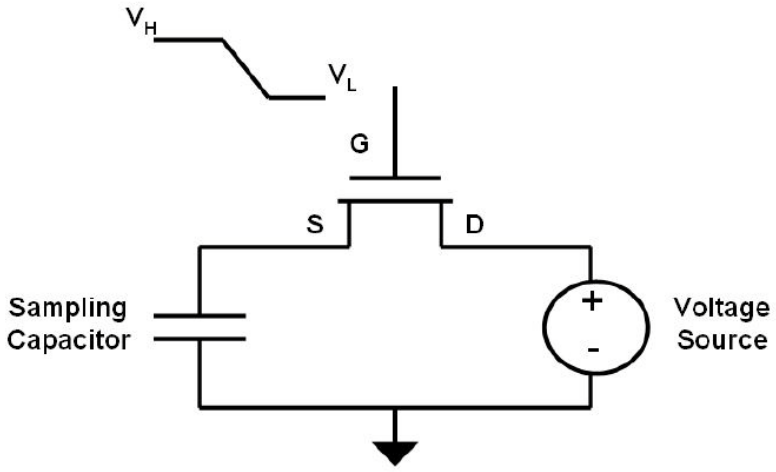

Figure 3.3. Charge injection and clock feedthrough occur in a switched-capacitor circuit when the gate turns off.

Current and switching time mismatch:

Since CMOS charge pumps usually have PMOS and NMOS as UP and DOWN switches, the switching time mismatch and the current mismatch dump additional charge to the loop filter. When the mismatch in the charge pump is known, it is important to reduce the turn-on time of the phase detector (PD).

The switching time mismatch is inherent to PDs with the single-ended charge pumps since the UP and the DOWN outputs have to drive PMOS and NMOS switches. In PLL-based frequency multipliers, spurious tones are generated by timing mismatch between I_{up} and I_{dn}. The switching time mismatch can be reduced by equalising the delay and the transition time of the UP-DN pulses from the PD to the charge pump circuit with the use of some carefully-designed buffers.

Current-level mismatch can be considered under static and dynamic sources. Static offsets can be avoided by using a current compensation scheme through a replica feedback and keeping the current source resistance high [18] [19]. In many cases, the static sources of spur generation, predictable and invariant in time, can be rather easily

removed with special circuitry. However dynamic spur sources, i.e. glitches on the loop filter, are more difficult to fully remove because they are created by time-varying effects such as charge sharing, clock feedthrough and charge injection [16].

3.2.2 Noise in VCO

Since the frequency of oscillation is a function of the tail current in each stage of the ring oscillator or ramp current in the relaxation oscillator, noise components in this current modulate the frequency, thereby contributing to phase noise. The current noise stems mostly from the MOS device electronic noise. Moreover, the frequency of an oscillator is also depended on the rail voltages (V_{dd} and V_{ref}). Voltage variations of the rail voltages are primarily caused by supply and substrate injected noise. As previously discussed in this research, we consider the voltage noise present on the two rail voltages (V_{dd} and V_{ref}) and current noise riding on top of the tail or ramp current to be the two major noise sources contributing to phase noise. Prior articles have reported techniques to effectively suppresses power supply and substrate noise by employing fully differential ring oscillators, which exhibit a good power supply and substrate rejection ratio (PSRR). Increasing the swing of the ramp voltage is another obvious method to

reduce power supply and substrate noise effects. Device noise is unavoidable. This thesis work provides a good prediction of the lower bound of phase jitter caused by device noise.

Since the charge pump is inactive as long as the PLL is locked onto the target frequency, the noise components of the VCO are the major issue in a PLL. Charge pump noise can be considered by a single noise source added to the input of the VCO. This allows calculating a symbolic expression for the PLL phase jitter.

3.3 Introduction of jitter

The noise manifests itself as jitter at the output of the PLL, primarily through various mechanisms in the voltage-controlled oscillator (VCO). PLL based frequency synthesizers are widely used in low cost, high precision IC solutions for data converters.

3.3.1 Why jitter matters

Clock jitter is probably the most obscure specification in data converters. It basically describes the timing errors in the sampling operation due to clock transition errors. In fact, the clock applied to the

data converter determines the timing of the samples produced from the input signal. Therefore, any clock disturbances must be minimized.

In any switch-capacitor circuit, sample and hold circuit or ADC, the clock defines the sampling process that normally takes place at the very first stage. An error in the sampled value cannot be corrected later because it is already attached the sampling sequence used for digitization and thus will impact the overall performance of the data converter system.

Clock disturbances can be classified as disturbances of amplitude and frequency. The latter one is also called time jitter. Any small disturbances to the amplitude of the clock have no effect or the overall performance because the switch is a binary device, which is either on or off as long as the fluctuations are below a certain threshold. But time jitter can have a huge and direct impact on the sampled signal and generates an irreversible error.

Therefore, time jitter is critical to the performance of data converters or any applications requiring sampling. The trend of data converters is to

increase sampling frequencies and increase resolution. This increases sensitivity to time jitter. Thus, being aware of how much jitter is acceptable for certain requirement of data converters is significant.

Assuming a jitter value of Δt on the sampling instant, the error produced is proportional to the derivative of the input signal [21] [22].

$$V_{error} = \Delta t \frac{dv_{in}}{dt} \tag{3.9}$$

For a sinewave of frequency f_{in} and amplitude A_{in}, the maximum error is

$$V_{error\ \max} = \Delta t \cdot A_{in} \cdot 2\pi \cdot f_{in} \tag{3.10}$$

In order to have this error below 0.5 LSB in an N-bit data converter with input range +/- A_{in}, the maximum value of the jitter is

$$V_{error\ \max} = \Delta t \cdot A_{in} \cdot 2\pi \cdot f_{in} \tag{3.11}$$

For example, for a 12-bit 100 MHz ADC with maximum bandwidth of 50 MHz, the peak to peak jitter specification is 0.8 ps. This is the time jitter requirement if we assume that the jitter is always the maximum. However, jitter statistics are typically similar to random noise.

Therefore, the jitter requirement stated in equation (3.11) is too restrictive.

3.3.2 Definitions of time jitter

We consider the output voltage V_{out} of an oscillator in the steady state. For an ideal oscillator, the period of the clock signal is T, but in reality, the period of the clock signal with phase noise is T_n. T_n varies with n as a result of noise in the circuit. This results in a deviation $\Delta T_n = T_n - T$. The quantity ΔT_n is an indication of jitter.

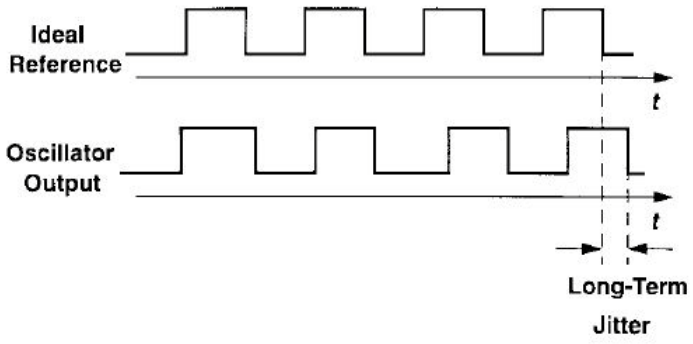

Figure 3.4. Definition for long term jitter.

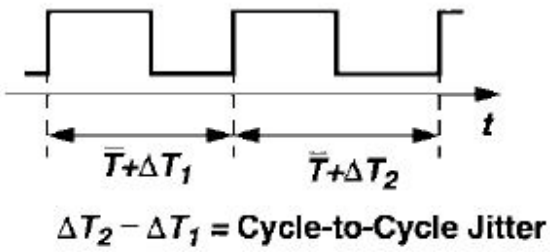

Figure 3.5. Definition for cycle to cycle jitter.

More specifically, long-term jitter

$$\Delta T_{long}(\mathrm{N}) = \sum_{\mathrm{n}=1}^{\mathrm{N}} \Delta \mathrm{T_n} \tag{3.12}$$

is often used to quantify the jitter of PLLs. Modeling the total phase error with respect to an ideal oscillator as illustrated in Figure 3.4.

Another figure of merit for oscillators is period jitter, defined as the timing error $\Delta \mathrm{T_n}$. Sometimes, the rms value of the period jitter is used to reveal the jitter performance of the oscillator or PLL circuit. The rms value of period jitter is defined as

$$\Delta T_{n_{RMS}} = \lim_{n\to\infty} \sqrt{\frac{1}{N} \sum_{n=1}^{N} \Delta T_n^2} \tag{3.13}$$

The period jitter describes the magnitude of the period fluctuations, but it contains no information about the dynamics.

The third type of jitter considered here is cycle-to-cycle jitter as illustrated in Figure 3.5. It is given by

$$\Delta T_{c\text{-}c} = \lim_{n\to\infty} \sqrt{\frac{1}{N} \sum_{n=1}^{N} (\mathrm{T_{n+1}} - \mathrm{T_n})^2} \tag{3.14}$$

$\Delta \mathrm{T_{c\text{-}c}}$ represents the rms difference between two consecutive periods.

3.3.3 Jitter measurement

Jitter can be measured directly in the time domain or indirectly via the frequency domain.

Time domain measurement

Low frequency jitter (kHz) can be measured by a high sampling rate oscilloscope with enough memory depth. Oscilloscopes can record and store more than one million cycles and some oscilloscopes have jitter analysis software tool installed. This allows calculating period jitter, cycle to cycle jitter or long term jitter in a straight-forward way. This method is very convenient. The only drawback is that a high sampling rate oscilloscope with jitter analysis tool is extremely expensive. An alternative is to carry out the jitter analysis using Matlab or any other programming language. This is a lower cost solution but consumes much more time and has a longer testing time.

Frequency domain measurement

Jitter of high frequency clock signals (MHz, GHz) is difficult to measure directly. In the frequency domain, the phase noise of a clock signal is its phase modulation due to the time domain clock variation

(time jitter), hence, it is quite straightforward to measure the phase noise of a clock signal and then convert phase noise power to jitter in the time domain. A common spectrum analyzer can then be used.

The clock signal of a data converter is often derived from a PLL. The spectrum of PLL jitter follows the shape illustrated in Figure 3.6. It is reasonably flat within the loop bandwidth, and rolls-off a higher frequencies. Therefore, most of the phase noise energy is located in the loop bandwidth. For simplicity, let us represent the clock as a sine wave of frequency F_s [23].

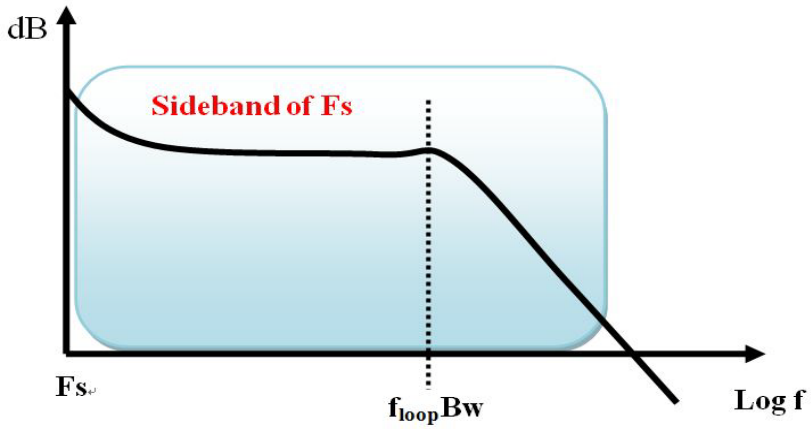

Figure 3.6. Typical spectrum shape of the clock jitter produced by a PLL.

$$V_{clock} = A\sin(2\pi \cdot \mathrm{F_s} \cdot \mathrm{t} + \phi(\mathrm{t})) \tag{3.15}$$

Where $\phi(\mathrm{t})$ is the phase noise in the time domain. Assume $\phi(\mathrm{t})$ is small,

$$V_{clock} \cong A\sin(2\pi \cdot \mathrm{F_s} \cdot \mathrm{t}) + \mathrm{A}\cos(2\pi \cdot \mathrm{F_s} \cdot \mathrm{t}) \cdot \phi(\mathrm{t}) \qquad (3.16)$$

The second term of the expression in (3.16) is the phase noise $\Phi(f)$ and appears as sidebands around the center frequency (Fs). The phase noise appears multiplied by a cosine at the clock frequency. It is often represented as L(f), or single-sideband phase noise power spectral density at the frequency Fs+f divided by the clock signal power $A^2/2$. It is called single-sideband because only one side of noise power is taken into account, so it includes only half the noise energy. Therefore, it is related to $\Phi(f)$ as:

$$L(\mathrm{f}) = 10\log(\frac{1}{2}\Phi^2(\mathrm{f})) \qquad (3.17)$$

$$\Phi(\mathrm{f}) = \sqrt{2 \cdot 10^{\frac{L(f)}{10}}} \qquad (3.18)$$

L(f) has units of dBc/Hz and corresponds to what is visible in a spectrum analyzer at offset frequencies within the bandwidth from the clock center frequency as shown in Figure 3.6. To obtain the total jitter from the spectral phase noise, the phase noise, power scaled by $1/2\pi$Fs, is integrated over frequency :

$$\Delta t_{rms} = \frac{1}{2\pi \cdot F_s}\sqrt{\int_0^\infty \Phi^2(\mathrm{f})\mathrm{df}} \qquad (3.19)$$

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Chapter 4

Introduction of Ultra-Low Power Design

4.1 The purpose of ultra-low power design

Advances in CMOS technology, communications, and low power circuit design techniques have spurred considerable interest in medical devices, a phenomenon which can potentially revolutionize the healthcare industry. Many kinds of medical devices are battery-operated, such as EMG/EKG data acquisition system, blood glucose meters, heart rate monitor and pacemakers. Low power building blocks are essential for them in order to maximize the battery lifetime [1].

The low power design is also an important objective for portable medical equipment such as implantable medical sensors [2] to reduce the system cost as an increased energy demand has to be covered by a higher battery capacity.

The trend of battery operated portable medical equipment renders

wireless biological signal acquisition of great interest for both industry and academic research. This is one reason why research for wireless body area networks have become a hot topic, recently and are considered emerging application for new generation healthcare and entertainment systems [3]. The major design challenge associated with the wireless body area network is to extend the lifetime of devices with limited energy sources. In other words, ultra low power design is the main concern and first priority.

4.2 The strategies for ultra-low power PLL design.

Nowadays, low jitter and low power are the most critical characteristics for a PLL design. An ultra low power design always affects the clock accuracy. So in designing a PLL, trade-offs need to be made for compromising between demand and performance. In this section, our emphasis is ultra low power design strategies for a PLL.

4.2.1 Low power consideration from circuit design.

Choice of VCO:

As we presented in Chapter 2, crystal oscillators, LC oscillators, ring

oscillators and relaxation oscillators are normally used in PLL circuit. Crystal oscillators and LC oscillators are able to provide a better jitter performance, but for low power and power-efficient considerations, ring oscillators and relaxation oscillator circuits are preferred.

Although ring oscillators and relaxation oscillators are less accurate, they exhibit excellent characteristics for ultra low power operation and relatively good precision when operated in the subthreshold region [4] [5] which we will discuss in section 4.2.2. Apart from low power consumption, they enable a small die area, since no external inductors and capacitors are needed. They require significantly less die area than LC and crystal oscillator and are more compatible with standard digital CMOS processes [6]. Furthermore, ring oscillators provide multiple output phases with a wide tuning range as required by some specific implantable electronic devices.

After the decision has been made to use a ring or relaxation oscillator to minimize power, we have to work on the VCO circuit structure for power-efficiency improvement. Power dissipation can be reduced directly by minimizing current consumption. In the proposed relaxation

oscillator, we reduce the number of comparators and current conducting branches in order to achieve an ultra low power dissipation.

A common relaxation oscillator structure comprises a capacitor that is charged by a constant current and is periodically discharged as soon as the capacitor voltage exceeds a certain threshold voltage [7] [8]. Previous implementations have used two comparators [9], while the proposed relaxation oscillator in this work contains only one comparator to reduce the current consumption.

A comparator current generator has also been implemented to provide a reference voltage in the proposed structure. This scheme shares the comparator current with the reference voltage generator. Such a current-sharing scheme reduces the number of current-conducting branches and leads to a lower current consumption.

Choice of loop filter

In this work, we have opted to use a second-order passive loop filter instead of an active loop filter (cf. Chapter 2) to further minimize the

power dissipation.

Choice of digital cells (phase detector, digital counter)

The digital cells of our PLL are a phase detector and a digital counter. To achieve the intended ultra-low power dissipation, all digital units are based on static CMOS design techniques.

In static CMOS design, each gate output is connected to either V_{dd} or V_{ss} at any instant in time. A static CMOS logic is a combination of two networks - the pull-up network and the pull-down network. Static CMOS gates have rail-to-rail swing, and dissipate no static power. The speed of the static CMOS circuits depends on the transistor sizing and the various parasitics that are involved with it. The problem with this type of implementation is that it has twice the capacitive loading, and uses both NMOS and PMOS transistors.

In contrast, in dynamic logic, there is not always a mechanism driving the output high (V_{dd}) or low (V_{ss}). In the most common version of this concept, the output is driven high or low during a distinct clock phase.

When the output is not actively driven, the high impedance prevents the charge to leak rapidly and keeps the voltage within some tolerance range. If only NMOS transistors are used in dynamic CMOS, the logic, when properly designed, can be twice as fast as static logic.

The main advantages of dynamic CMOS logic are increased speed and reduced implementation area. However, it consumes more power than static logic CMOS logic. For any design to feature low power as its first consideration, static CMOS is a better solution.

Use different voltage supplies for analog and digital parts

Using different supply voltages in a system to reduce power has been proposed and published over the past decade. An extra voltage regulator is normally added to keep the generated supply voltage internally stable. A lower supply voltage is used for digital cells to decrease power dissipation. Since the extra circuitry for the different supply voltage increases the design complexity and may cause more noise, a trade-off needs to be analyzed along all the performance parameters.

4.2.2 Low power consideration from transistor operation region.

A MOS transistor has three operation regions. They are triode, saturation and subthreshold region (or weak inversion). In recent years, subthreshold operation has gained a lot of attention due to its ultra low power consumption. It has also been shown that by optimizing the device structure. Subthreshold power consumption can be further minimized while improving performance. Consequently, subthreshold circuit design is very promising for ultra low-energy applications as well as for high performance parallel processing.

The device equations presented for MOS transistors below are for triode and saturation region operations, respectively.

$$I_d = \mu_n C_{ox} \frac{W}{L} \left((\underbrace{V_{GS} - V_{th}}_{V_{eff}}) V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{4.1}$$

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (\underbrace{V_{GS} - V_{th}}_{V_{eff}})^2 \tag{4.2}$$

Equation 4.1 pertains to an NMOS transistor operated in the triode region and voltage and current relationship for an NMOS transistor in

saturation region is shown in equation 4.2. Both equations are based on the assumption that V_{eff} is greater than 50 mV or so. If this is not the case, the accuracy of the square-law equations is poor, and the transistor is said to be operating in the subthreshold region. In this region, the transistor is more accurately modeled by an exponential relationship between its control voltage and current, somewhat similar to a bipolar transistor. In the subthreshold region, the drain current is approximately given by the exponential relationship

$$I_d = I_{d0}(\frac{W}{L})e^{(qV_{GS}/nKT)} \tag{4.3}$$

where n is between 1 to 2, and V_s has been assumed to be zero. Note that $V_{ds} < 75$ mV. The constant I_{d0} might be around 20 nA.

Sub-threshold circuits operate with a supply voltage that is less than the threshold of the transistor—far below traditional levels and therefore, the transistor operates essentially on leakage, leading to a very low power consumption. Running at these nonstandard operating points limits performance. This may remain acceptable for low-to-medium cost applications given the substantial increase in the corresponding energy efficiency. As power relates quadratically to the

supply voltage, reducing the voltage to these ultra-low levels results in a dramatic reduction in both power and energy consumption in systems.

However, since the subthreshold leakage current is used as the operating current in subthreshold operation, these circuits cannot be operated at very high frequencies, because only small leakage currents are available to charge and discharge capacitors. In addition, matching between transistors suffers. It is now dependent primarily on transistor threshold voltage matching which is a temperature and process sensitive parameter. Thus, transistors will be operated in the subthreshold region only for ultra-low power and relatively low frequency applications.

The potential for minimizing energy at the cost of speed defines the following set of applications for which subthreshold circuits are well suited.

- Wireless senor nodes
- RFID tags
- Medical equipments (hearing aids, pace-maker, wearable implants)

Those applications are dominated primarily by the need to minimize energy consumption and increase battery life time. Speed is a secondary consideration and so, subthreshold circuits are considered a better solution.

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Chapter 5

Building blocks of PLL

5.1 Phase frequency detector

The phase frequency detector (PFD) is used to detect phase and frequency differences between two signals. If PFD is implemented in PLL circuit. Its two inputs are the reference signal and the PLL feedback signal. The output signal is typically a voltage. The voltage can be used directly in the next stage or converted to a current.

5.1.1 XOR (Exclusive OR)

The simplest phase detector is an XOR (Exclusive OR) gate. Figure 5.1(a) indicates XOR gate and relationship between output difference and input phase difference. Figure 5.2(b) shows the input and output signals of the XOR. The two inputs have to be 50% duty cycle signals to achieve a correct phase frequency detection.

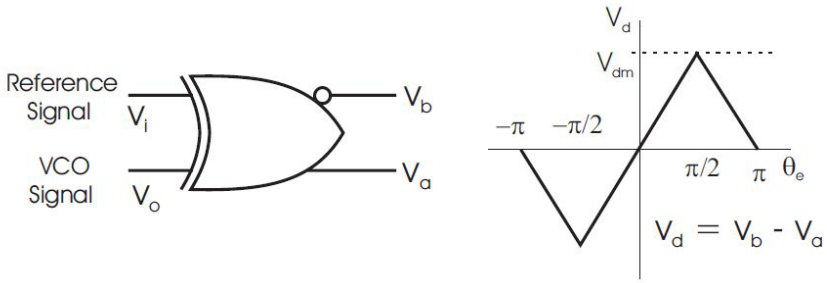

Figure 5.1(a). XOR phase detector.

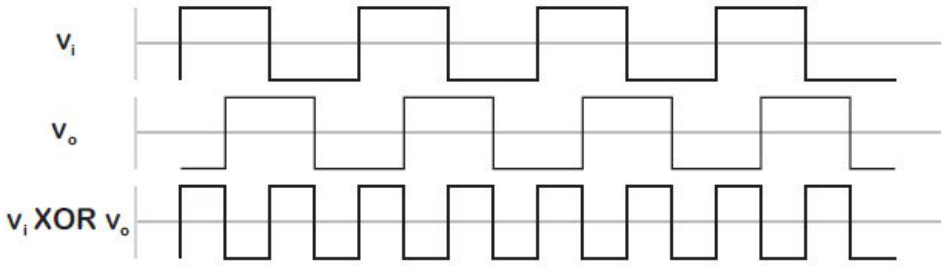

Figure 5.1(b). XOR phase detector waveform.

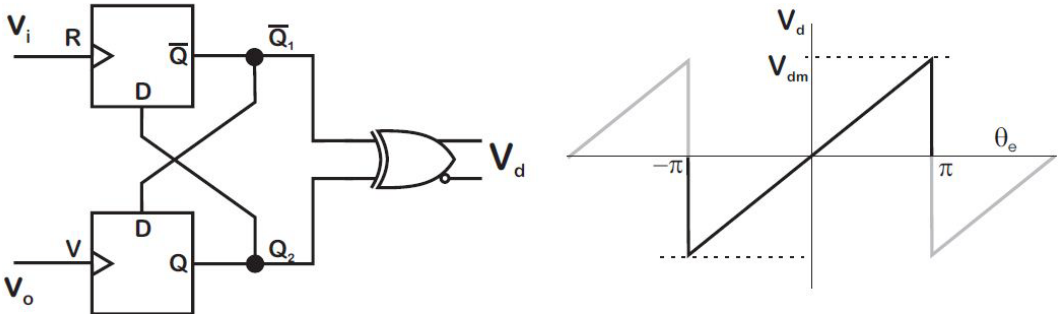

Figure 5.2. Two-state PFD.

5.1.2. Two-state PFD

Figure 5.2 presents a two-state PFD circuit. Two-state PFDs feature two additional flip flops. This solution renders the PFD sensitive to the

rising edges of the input signals only rather than to their duty cycles. Moreover, the linear region of the XOR is only $\pm\pi/2$, while the two-state PFD realizes a range to $\pm\pi$ as demonstrated in Figure 5.2.

5.1.3 Classical third-state phase detector

To be able to increment, maintain, or decrement the voltage controlled oscillator (VCO), designers prefer a phase detector (PD) with a ternary output. The tri-state phase detector (PD) with charge pump, presented in Figure 5.3, is extremely popular and is used in frequency synthesis, motor control, etc. The phase detector consists of two D filp flops (DFFA and DFFB) and an AND gate. Two current sources (I_p and I_d) and two switches (S1, S2) compose the charge pump. The charge pump can be viewed as a three-position switch controlled by the phase detector.

1. Position 1: Q_a is digital 1 and Q_b is digital 0; switch S_1 is on and S_2 is off. Current I_p goes through S_1 to charge C_z in the loop filter and the control voltage goes up.

2. Position 2: Q_a is digital 0 and Q_b is digital 1; switch S_1 is off and S_2 is on. Charge pump sinks current I_d from loop filter capacitor and

the control voltage drops down.

3. Position 3: Q_a is digital 0 and Q_b is digital 0; S_1 and S_2 are both off. The PLL is settled and the control voltage is remains constant.

The current phase curve in Figure 5.3 shows that the behavior of I_{out} with respect to the actual phase shift between A and B. Figure 5.4 reveals the PD output signals when the inputs do not match phases.

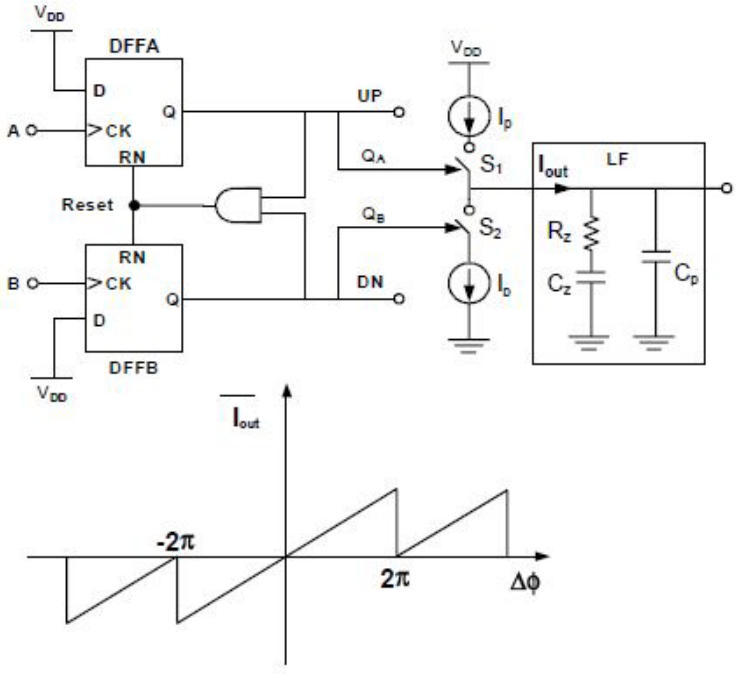

Figure 5.3. Block diagram of classic tri-state phase frequency detector with charge pump current phase.

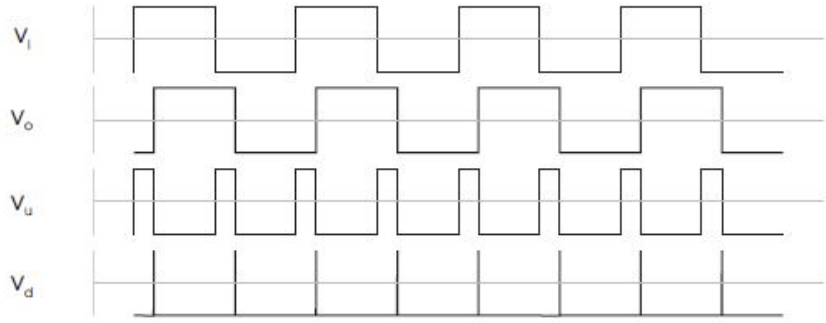

Figure 5.4. Input and output signals of tri-state PD.

Since only the leading edges of two inputs of the PD matter, their duty circles do not have to be 50%. This desensitizes the PLL feedback signal and makes the reference clock generator design a lot earlier.

5.1.4 Design in this work

In this project, we have designed a tri-state PFD as presented in Figure 5.5 with much less transistors than a classical third-state phase detector. It is an efficient implementation of a 3-way PD circuit based on static CMOS techniques. The 3 digital outputs created by this circuit are **up** (increment), **dwn**, (decrement) and **Nup**, **Ndwn** (maintain). These three control digits are used to control generate the control voltage for the VCO via charge pump and loop filter.

This control process is achieved by means of a charge pump and a loop

filter, which will be introduced in the next section. The schematic of a charge-pump and loop filter is shown in Figure 5.3. The charge-pump sources or sinks current based on the **up** and **dwn** signals. The charge-pump converts the two output voltages of the PD into a current. This current charges and discharges the capacitor in the loop filter and varies the control voltage of VCO. The 2 input voltages of the depicted phase frequency detector circuit, i.e. $\mathbf{V_{ref}}$ and $\mathbf{V_{fb}}$, are square waves with arbitrary duty cycles. The input and output signals for the PD are illustrated in Figure 5.6.

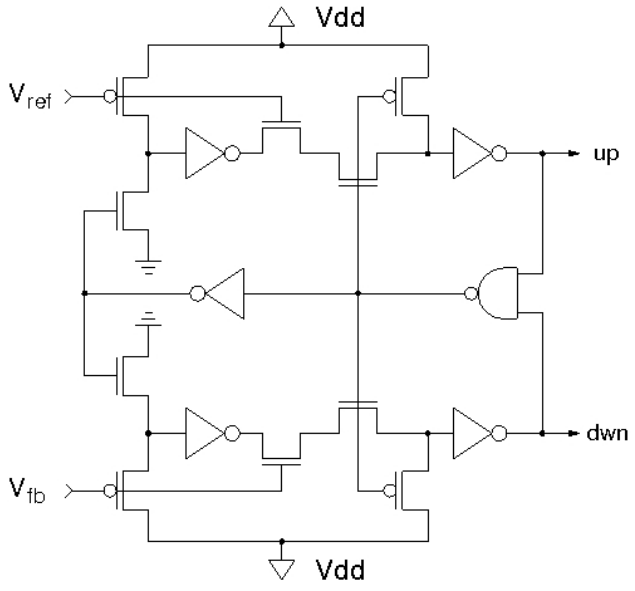

Figure 5.5. Ternary PD in CMOS technology.

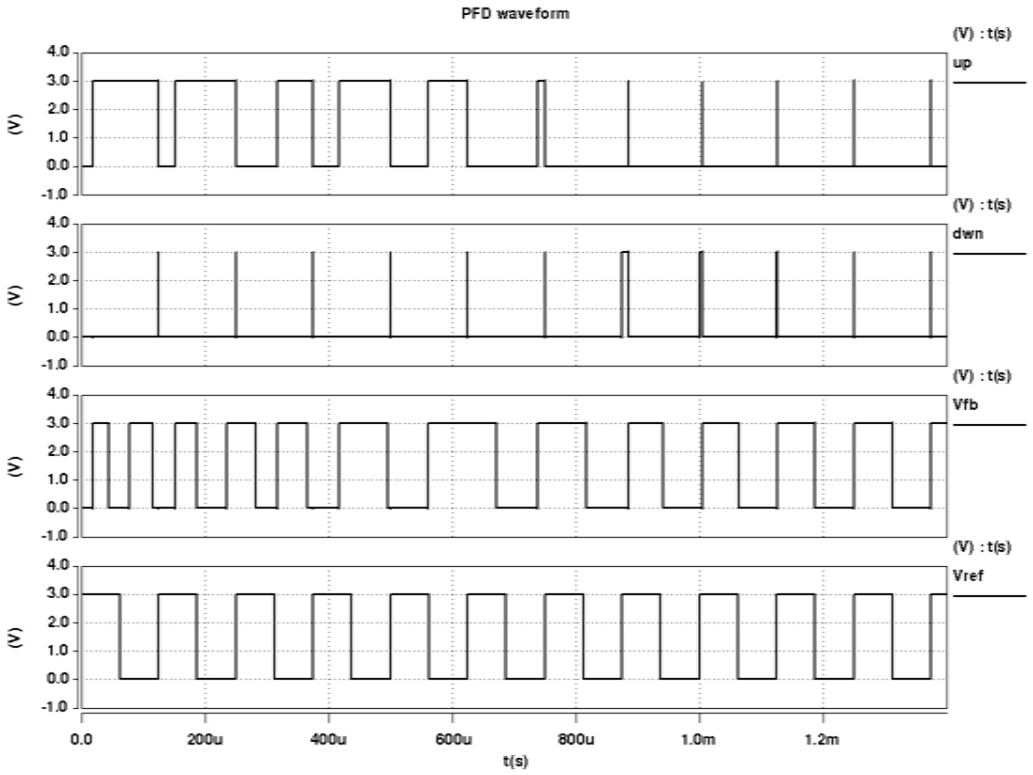

Figure 5.6. Phase Frequency detector waveforms.

Some of the characteristics of a phase frequency detector are:

1) The output of the phase frequency detector depends on both the phase and the frequency of the inputs.
2) Since the two-state and tri-state PFDs compare only the rising edges of the waveforms, it is not necessary for the VCO output to have a 50% duty-cycle.
3) A PLL using a PFD and charge-pump will not lock on harmonics as both the phase and the frequency are compared and matched. As a result, the PLL can operate over the entire VCO frequency range.

4) The ripple in the output frequency due to modulation of the control voltage is eliminated.

5.2 Loop filter (LF)

A loop filter is often used in PLLs and synthesizers, not only for converting the current from the charge pump to the control voltage for the VCO, but also for filtering out noise coming from the input reference signal to the control voltage of the VCO, otherwise, unacceptably high spurious tones will appear in the PLL output spectrum [5]. Active filters and passive filters are two major classifications. Because an active filter consumes a lot more power and ejects more noise than passive filter, we have chose a passive loop filter to achieve low power, low jitter purpose for this work. However, as can be seen in the layout chapter, the loop filter capacitor occupies more than 50% of the area of the entire PLL. So, a passive loop filter is easier to implement but needs a lot more area than an active loop filter.

This section presents second-order and third-order loop filters. As shown in Figure 5.7, an input pulse signal **e(t)** goes through the loop filter with high frequency components and noise, but the loop filter

blocks out all the high frequency parts and noise. Consequently, a nearly constant voltage **v(t)** is left as the VCO control voltage.

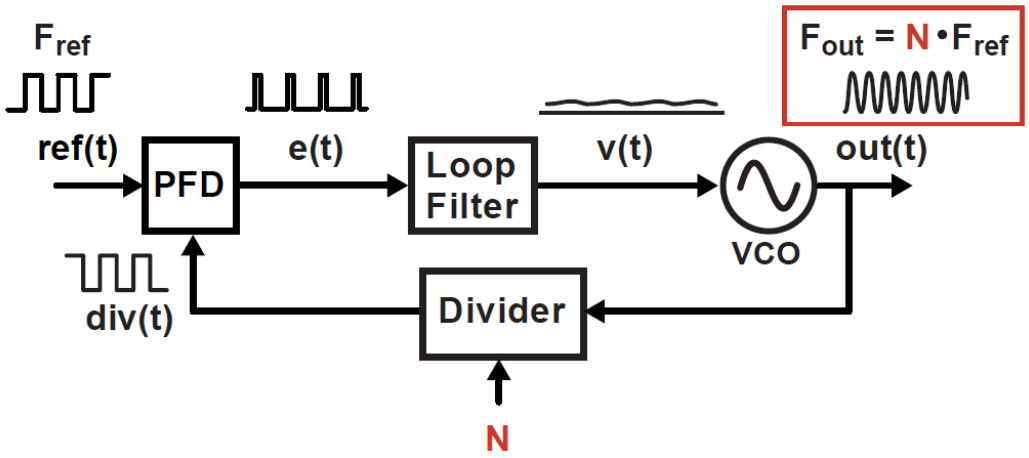

Figure 5.7. PLL diagram with input and output signal of each block.

5.2.1 Second order loop filter

The loop filter in an all-digital PLL is typically realized by a charge pump. The standard single-ended passive loop filter configuration for a charge pump PLL is shown in Figure 5.8. The serial RC_1 section forms a first-order lowpass filter, which (partially) removes the higher frequency components in the (digital) phase detector output $\mathbf{V_{ctl}}$. Capacitor C_2 has been added to prevent vertical steps in the control voltage of the VCO, which would cause undesired glitches and sudden frequency changes in the VCO output [1]. The unexpected control

voltage ripples are illustrated in Figure 5.9 and can be eliminated effectively by shunt capacitor C_2. C_2 is the parasitic capacitor of C_1 and the capacitance has to be less than $C_1/10$ for stability and larger than $C_1/50$ for low jitter goal.

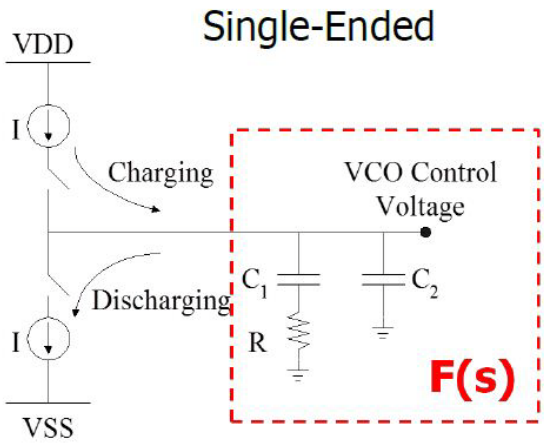

Figure 5.8. Single-ended second order loop filter.

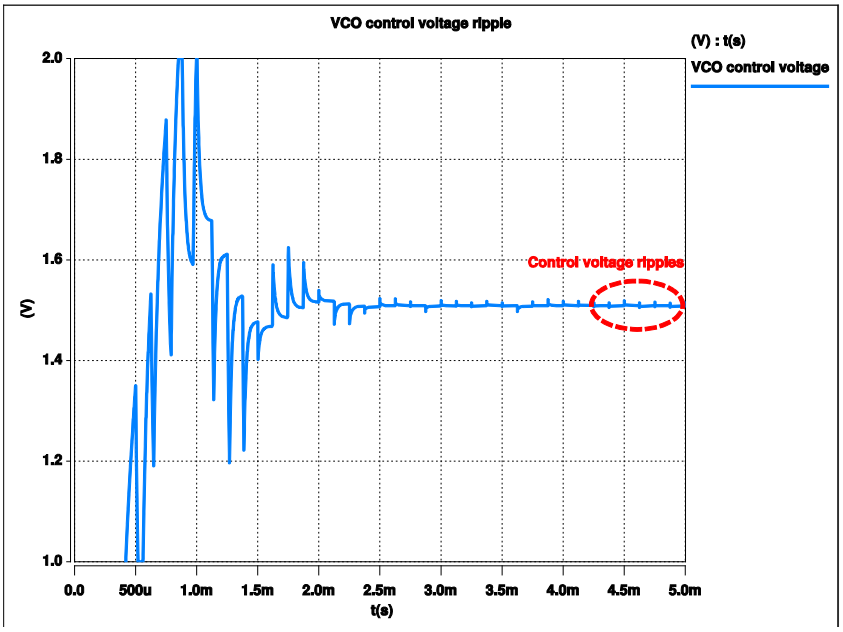

Figure 5.9. Control voltage ripple.

If we neglect secondary capacitor C_2, the transfer function F(s) is :

$$F(s) = \frac{R(s + \frac{1}{RC_1})}{s} = \frac{1 + RC_1 S}{C_1 S} \tag{5.1}$$

It has one zero at $f_z = 1/2\pi RC_1$ and one pole at $f_p = 0Hz$.

With C_2, the passive loop filter in Figure 5.8 is a second order filter. The transfer function F(s) is

$$F(s) = \frac{\frac{1}{C_2}(s + \frac{1}{RC_1})}{s^2 + \frac{s(C_1 + C_2)}{RC_1 C_2}} = \frac{1 + RC_1 S}{RC_1 C_2 S^2 + (C_1 + C_2)S} \tag{5.2}$$

It has one zero at $f_z = 1/2\pi RC_1$ and two poles at

$$f_{p1} = 0Hz$$

$$f_{p2} = \frac{C_1 + C_2}{2\pi RC_1 C_2} \tag{5.3}$$

Some designers have developed a fully differential charge pump second-order loop filter for a fully differential dual-PLL as shown in Figure 5.10. However, this design causes severe mismatch issues.

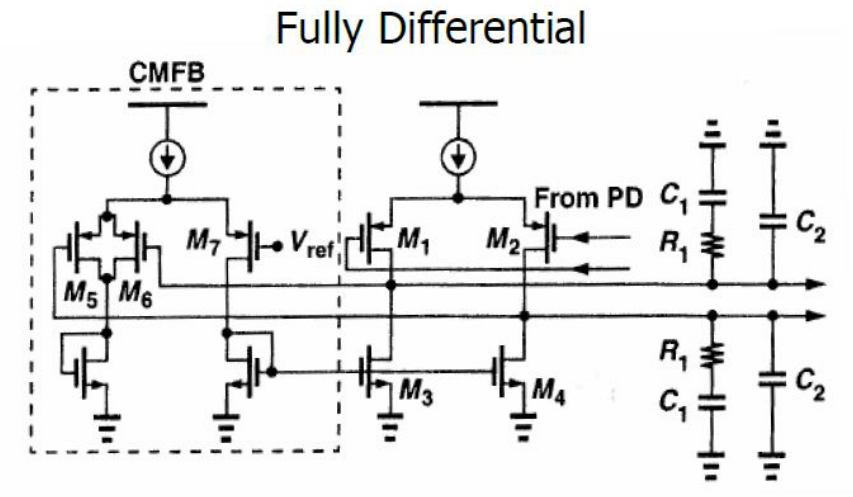

Figure 5.10. Differential second-order loop filter.

In this work, a charge pump loop filter has been implemented as shown in Figure 5.11. It is essentially a capacitor C_1 that is charged or discharged by a constant reference current. C_2 is typically selected to be about one-tenth the value of the filter capacitor C_1. A current sources the provide bias voltages $\mathbf{V_{b\text{-}p}}$, $\mathbf{V_{b\text{-}n}}$.

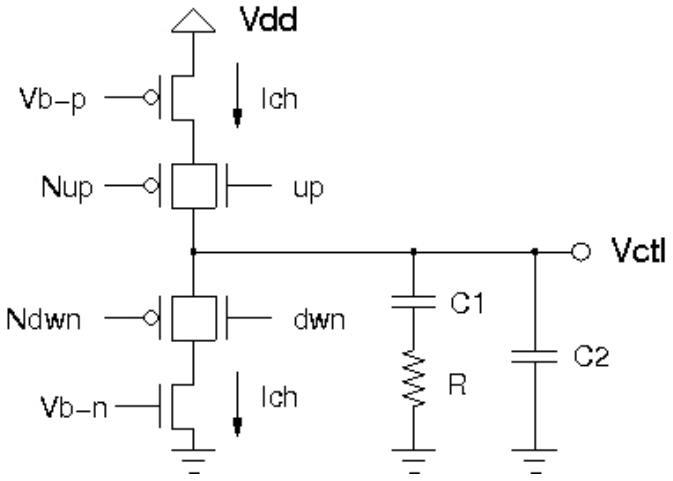

Figure 5.11. Charge pump with ternary control.

To minimize phase jitter induced by external noise, the loop bandwidth should be made as narrow as possible. On the other hand, to minimize the transient error due to signal modulation, or to minimize the output jitter due to internal oscillator noise, or to obtain best tracking and acquisition properties, the loop bandwidth should be made as wide as possible. Unfortunately, the loop bandwidth is affected by many process technology factors and is constrained to be well below the lowest operating frequency for stability. These constraints can cause the PLL to have a narrow operating frequency range and poor jitter performance.

The designer thus has to carefully weigh the pros and cons of selecting various sets of filter parameters. Based on the intended output frequency range of 10-150 kHz, we have decided on the following design compromise: C_1=25 pF, C_2=2.5 pF and R=8 MΩ.

The selected resistor and capacitor values are rather large for an area effective on-chip implementation. Some designers might therefore decide to keep them off chip to be able to readily adjust the tuning range and gain more control over the PLL locking characteristics.

Conversely, external components are rather costly and render the implementation more susceptible to noise injections and other parasitic effects. We have opted to realize the charge pump with on-chip components. To minimize circuit area, we have realized the large damping resistor of 8 MΩ by a very long n-channel device operated in the ohmic or triode region. While this implementation requires approximately 50 times less area than a passive resistor formed by the high resistive layer offered by the available 0.5um CMOS process, it is not perfectly linear and acts more like a distributed RC line than a simple resistor. However, as will be shown in the circuit simulation chapter, it does not severely alter the loop settling behavior. To prevent additional distortion, we have realized the filter capacitor C_1 as a passive element using the poly1-poly2 capacitor option offered by the chosen CMOS process. The charge-discharge current I_{ch} of the charge pump has been selected to be slightly smaller than 100 nA.

5.2.2 Third-order loop filter

In wireless communications, current switching noise in the dividers and the charge pumps at the reference rate, f_{ref}, may cause unwanted FM sidebands at the RF output. The phase detector comparison

frequency is generally a multiple of the RF channel spacing. These spurious sidebands can cause noise in adjacent channels. Additional filtering of the reference spurs is often necessary. This is usually the case in today's TDMA digital cellular standards, the sub-millisecond lock times necessary for switching between channel frequencies makes a relatively wide loop filter mandatory. For these performance critical synthesizer applications, a third-order loop filter (Figure 5.12) can be used to further suppress ripples at its output, which is also the control voltage of the VCO.

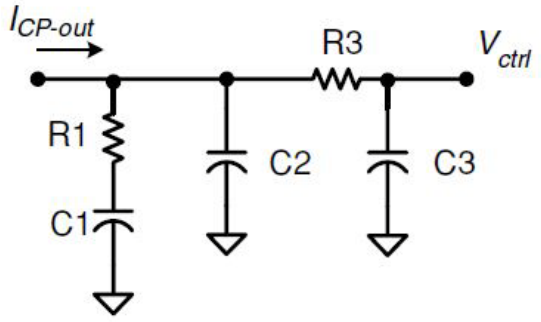

Figure 5.12. Third-order passive loop filter.

With one more pole being added, the transfer function F(s) of the loop filter becomes:

$$F(\mathrm{s}) = \frac{\mathrm{V_{ctrl}}}{\mathrm{I_{cp\text{-}out}}} = \frac{k'}{s}\frac{1+s\tau_z}{1+s\tau_{p2}} \cdot \frac{1}{1+s\tau_{p2}} = \frac{1+s(\mathrm{R_1C_1})}{\mathrm{s(C_1+C_2)(1+sR_1(C_1 \,||\, C_2))(1+sR_3C_3)}} \tag{5.4}$$

where:

K’ is the time constant of integration equal to $1/(C_1+C_2)$;

T_z is the time constant that provides a stabilizing zero to the loop which is equal to R_1C_1.

T_{p1} and T_{p2} are the time constants of the pole that suppress the tones of the reference clock and its higher harmonics. The time constant of T_{p1} equals $R_1C_1C_2/(C_1+C_2)$, while T_{p2} equals R_3C_3.

5.3 Voltage control oscillator (VCO)

The VCO is arguably the most critical block, since it decides about the frequency range and exerts the strongest influence on settling behavior as well as frequency and phase stability. This solution presents an ultra-low power low frequency relaxation oscillator and a ring oscillator and high frequency ring oscillator.

5.3.1 Relaxation oscillator

Since our target output frequencies lie in the extended audio range (10-150 kHz), we have opted for a current controlled relaxation oscillator. This solution allows us to minimize size and power

independently. Figure 5.13 depicts the proposed VCO circuit.

Figure 5.13 and Figure 5.14 show our relaxation oscillators with a complementary comparator to terminate the ramp. We have implemented two slightly different versions of the depicted VCO. In the first version (VCO1) as depicted in Figure 5.13, the comparator reference voltage, i.e., the gate voltage of transistor m3, has been connected to the common gate voltage of mb3 and mb4, while the second implementation (VCO2) utilized the lower common source voltage of the two biasing transistors as depicted in Figure 5.14.

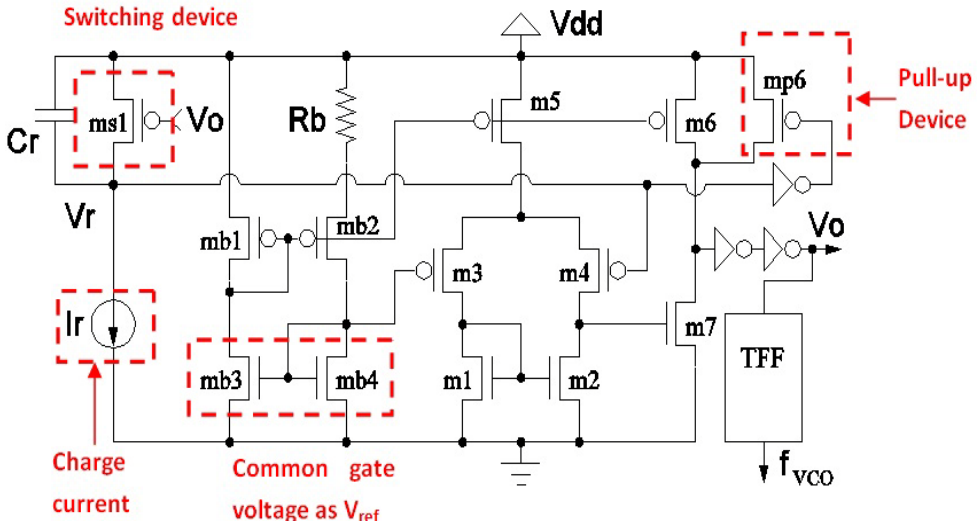

Figure 5.13. VCO1 with 2.4V swing.

To achieve the desired low frequency operation, the capacitor C_r of the

VCO is charged by a very small (voltage controlled) current ranging from approximately 2-74 nA. This creates a negative ramp ($\mathbf{V_r}$), which continues to decrease until $\mathbf{V_r}$ matches the reference voltage $\mathbf{V_{ref}}$. As soon as $\mathbf{V_r}$ drops below $\mathbf{V_{ref}}$, the comparator, realized by devices m1-m7, creates a short negative pulse, which resets $\mathbf{V_r}$ to $\mathbf{V_{dd}}$ by activating the switching device ms_1. To speed up the relatively slow comparator recovery time from its output low state to the (typical) output high state, we have added a servo loop consisting of a long-channel inverter (to minimize power) and an additional p-channel pull-up device (mp6) acting in parallel to the current mirror device m6. If we denote the very short reset phase of $\mathbf{V_r}$ by $\mathbf{T_{rst}}$, we can compute the period of the resulting sawtooth waveform as follows [3]:

$$T_{saw} = \frac{C_r}{I_r}(V_{dd} - V_{ref}) + T_{rst} \qquad (5.5)$$

Since T_{rst} will be on the order of a few ns while T_{saw} will be in the μs range, the slope of $\mathbf{V_r}$ can be approximated by the ratio $I_r/C_r=(V_{dd}-V_{ref})/T_{saw}$.

To maximize the sawtooth swing and with it the noise immunity, the

common source input pair of the comparator has been realized by p-channel devices. This extends the common-mode input range down to ground. $\mathbf{V_{ref}}$ could therefore be as small as the saturation voltage of the n-channel current mirror device (approximately 100 mV). In VCO1, we have conveniently utilized the common gate voltage of the 2 n-channel current source elements mb3 & mb4 as the reference voltage. $\mathbf{V_{ref}}$ is therefore almost identical to the threshold voltage of these 2 transistors. Combining the 3 V supply with the nominal n-channel threshold voltage of the chosen 0.5 μm CMOS process yields a sawtooth swing of about 2.4 V.

Selecting a p-channel rather than an n-channel comparator input pair is also beneficial with regard to flicker noise, since p-channel devices tend to suffer inherently less from these random charge carrier combinations than their n-channel counterparts. Furthermore, it provides for a higher negative slew rate and thus minimizes the comparator latency [2], [4].

A toggle flip-flop (TFF) converts the short negative voltage spike

produced by the comparator, i.e., $\mathbf{V_o}$, into a square wave with a 50% duty cycle. The VCO output frequency is therefore:

$$f_{VCO} = \frac{1}{2T_{saw}} \tag{5.6}$$

The ideal sawtooth swing and the VCO output frequency f_{VCO} are related as follows:

$$V_{dd} - V_{ref} = \frac{I_r}{C_r} T_{saw} = \frac{I_r}{C_r} \frac{1}{2 f_{VCO}} \tag{5.7}$$

As illustrated in Figure 5.13, the VCO is biased by a supply insensitive current source formed by transistors mb1, mb2, mb3, mb4 and resistor R_b. To obtain a sufficiently short comparator response time, we have selected the nominal tail current of the differential input pair to be 80 nA .

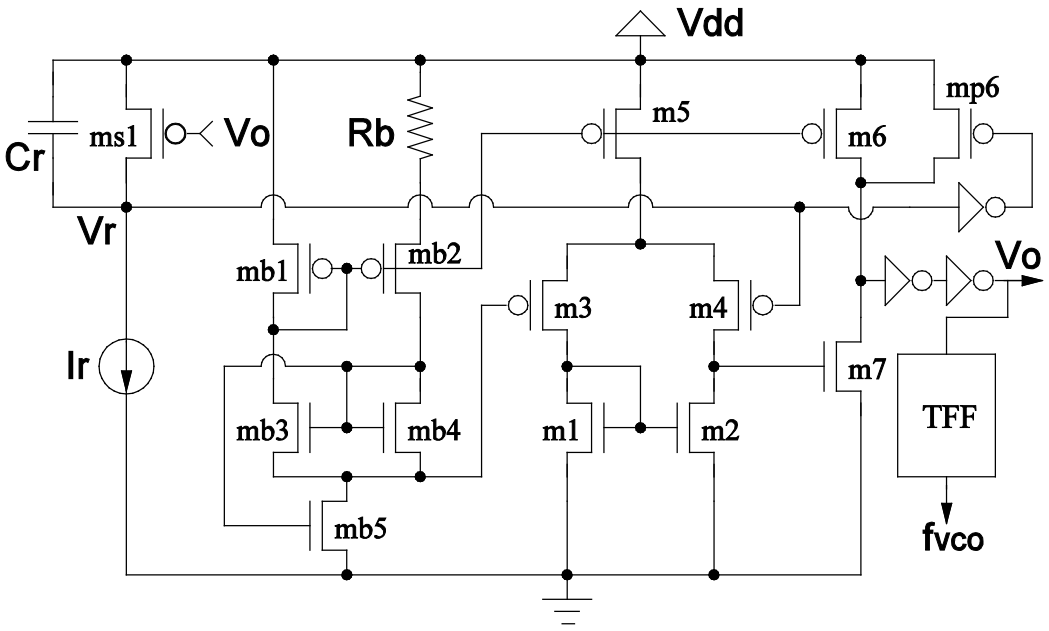

Figure 5.14. VCO2 with 2.85 V swing.

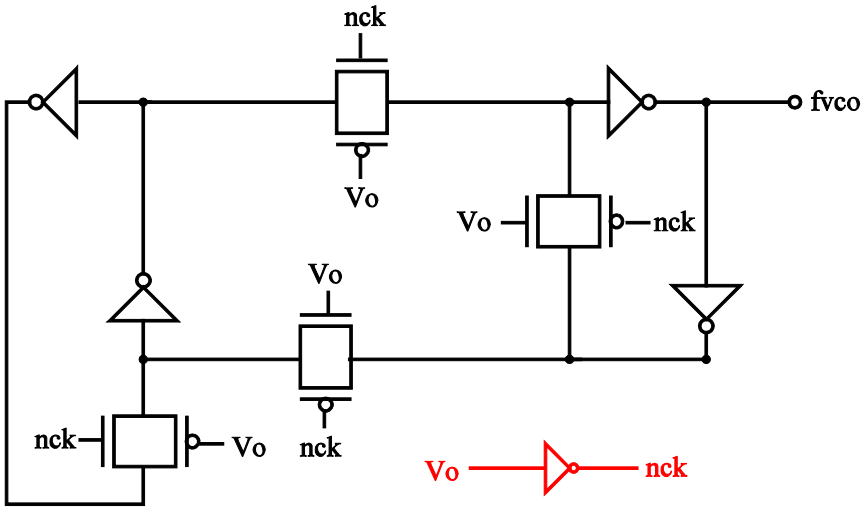

Figure 5.15. TFF for VCO circuit.

Figure 5.15 presents the transistor level design of the toggle flip flop (TFF) in Figure 5.13 and 5.14. As previously mentioned, the first implementation (VCO1) connects $\mathbf{V_{ref}}$ directly to the common gate

voltage of the biasing transistor pair mb3 & mb4. Utilizing a 3 V supply thus yields a sawtooth swing of about 2.4 V. In the second implementation (VCO2) as illustrated in Figure 5.14, mb5 has been sized to realize a drain potential of approximately 0.15 V to maximize the swing of the sawtooth voltage $\mathbf{V_r}$ to 2.85V. Our VCO circuits yield a very high positive power supply rejection (> 40 dB), but suffers from a rather poor ground noise protection (0.5 dB). Table 5.1 lists the critical performance parameters of the comparator circuit (m1-m5) depicted in both VCO circuits.

Table 5.1. Comparator performance parameters

Differential Mode Gain @ 10 kHz	75 dB
Common Mode Gain @ 10 kHz	-9.5 dB
Propagation Delay (T_{saw}=3.5 us)	186 ns
Propagation Delay (T_{saw}=35 us)	435 ns
Input referred thermal Noise V_{nth}	162 nV/Hz$^{1/2}$
Power Dissipation (V_{dd}=3 V)	700 nW

Figure 5.16 shows sawtooth wave V_r, comparator output V_o and VCO

output f_{vco}. V_o is a pulse signal with a very narrow negative pulse width. Therefore, a toggle flip flop is necessary for relaxation oscillator to converter the pulse to a 50% duty cycle square wave of frequency f_{vco}. Figure 5.17 and 5.18 show VCO frequency versus control voltage and power dissipation respectively. If the control voltage is increased, the bias current I_r will decrease in accordance with the voltage to current converter design that will be introduced in section 5.4. According to formula (5.5), the VCO output frequency is proportional to I_r, it is thus is inverse- proportional to the control voltage. As displayed in Figure 5.17, the relationship between control voltage and VCO output frequency is fairly linear and the power dissipation increases linearly as the frequency. The ultra-low power VCO consumes 0.9-1.35 μW over 24-120 kHz frequency range as shown in Figure 5.18.

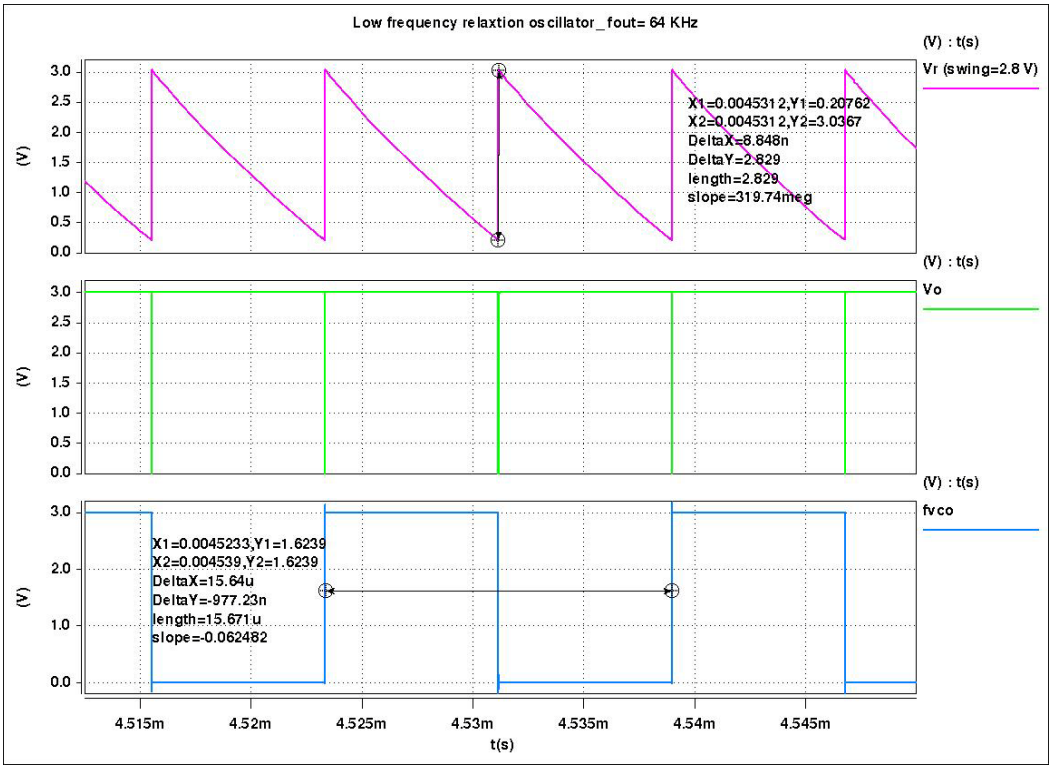

Figure 5.16. Simulation results for relaxation oscillator (10-150 kHz).

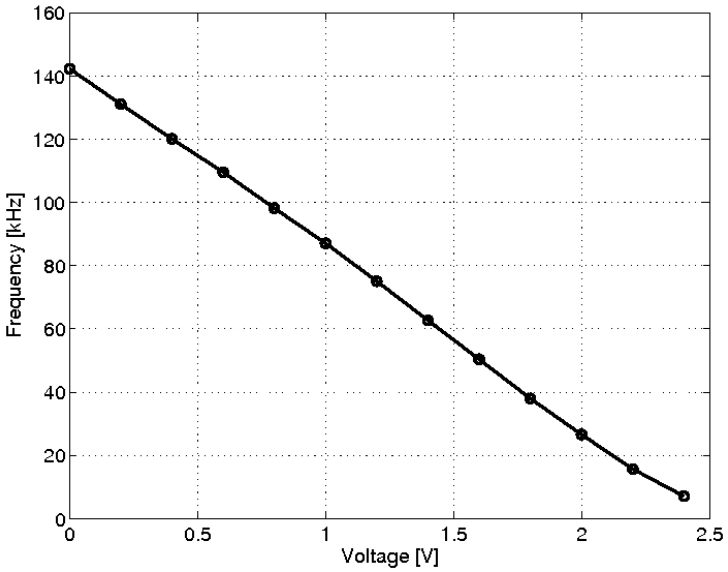

Figure 5.17. VCO frequency versus control voltage.

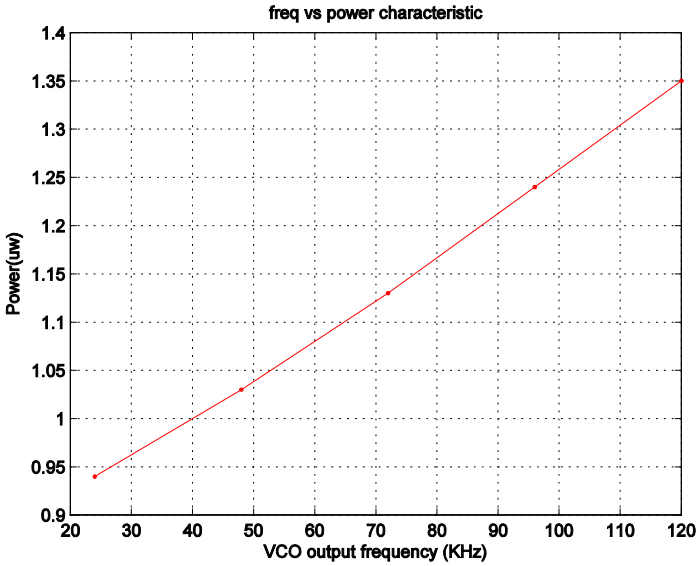

Figure 5.18. VCO output frequency versus VCO power dissipation.

The reason why we have implemented two versions of the VCO is that the lower reference is expected to minimize the influence of noise injected from substrate or V_{dd}. We prove this conclusion theoretically in this chapter and will verify it through physical testing results later. A further discussion about noise and noise reduction will be given in the jitter analysis chapter.

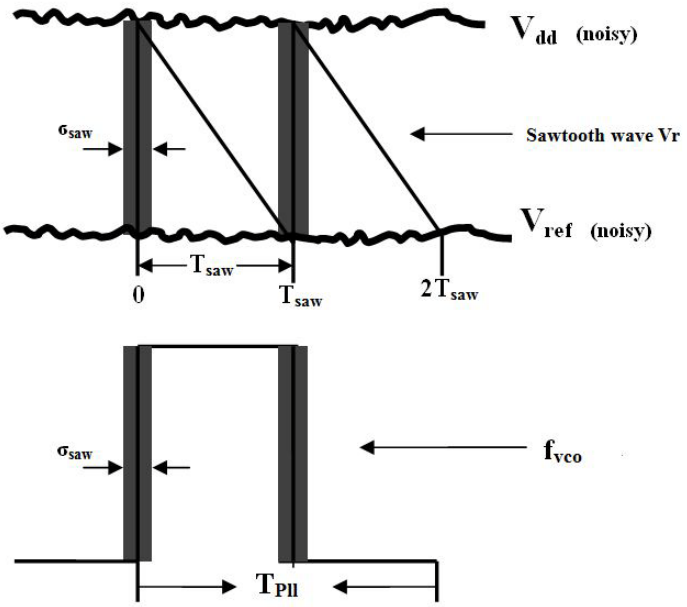

Figure 5.19. Noise and period jitter of sawtooth wave.

As shown in equation (5.5), all parasitic signal components affecting power supply and reference frequency $\mathbf{V_{ref}}$ will provide an undesired VCO output period variation in time domain. If the total noise voltage riding on $\mathbf{V_{dd}}$ and $\mathbf{V_{ref}}$ is represented by an equivalent differential input noise voltage $\mathbf{V_{n,}}$ we can approximate the variance of the subsequent comparator transitions by

$$\sigma_{saw} = \frac{V_n T_{saw}}{V_{dd} - V_{ref}} \tag{5.8}$$

A complete cycle of the square wave output of the VCO consists of two sawtooth periods (comparator transitions) and the disturbing signals present during two consecutive comparator transitions are

statistically independent.

If we assume the jitter of a PLL output is only caused by variation of the VCO output signal, the PLL's jitter T_J becomes:

$$T_J = \sqrt{\sigma_{saw}^2 + \sigma_{saw}^2} = \sqrt{2}\sigma_{saw} \qquad (5.9)$$

Therefore, maximazing the voltage swing ($\mathbf{V_{dd}}$-$\mathbf{V_{ref}}$) will minimize the influence of $\mathbf{V_n}$ on the period of the PLL output.

5.3.2 Ring oscillator

Most high-frequency VCOs are based on some form of current controlled or current starved ring oscillator. In this section, we implement a single-ended ring oscillator and a fully differential oscillator aimed at a relative low frequency range (10-150 kHz) and a high frequency range (10-100 MHz), respectively. The formula for ring oscillator frequency is:

$$f_{osc} = \frac{I_{bias}}{2 \cdot N \cdot C_{tot} \cdot V_{swing}} \qquad (5.10)$$

where:

I_{bias} : the bias current for each stage

N: the number of stages

C_{tot}: the load capacitance for each stage

V_{swing}: the peak to peak voltage of each stage's output voltage.

A. Low speed single-ended ring oscillator (10-150 kHz)

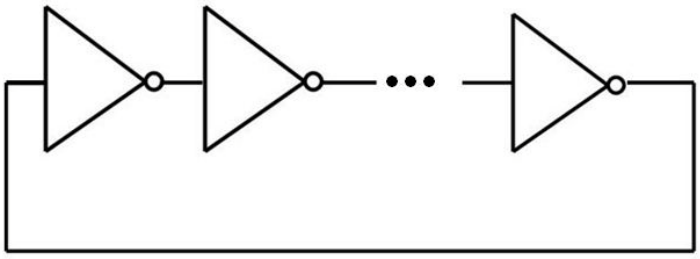

Figure 5.20. Conceptual single-ended ring oscillator.

Typically, the ring oscillator is formatted by a closed loop chain of inverters. In single-ended ring oscillators, each stage is an inverter formed by a pair of complementary transistors (PMOS and NMOS).

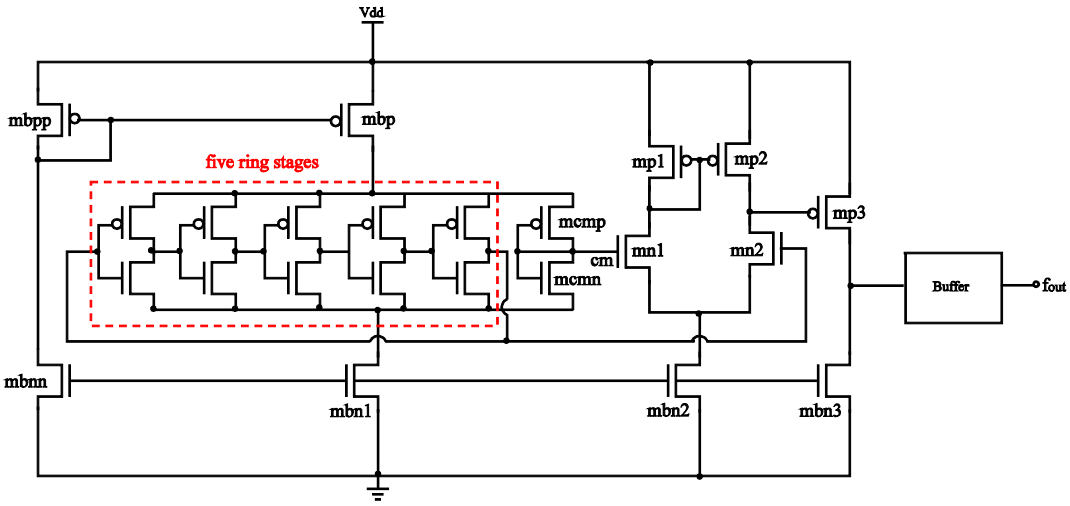

Figure 5.21. Practical low frequency 5-stage current starved ring oscillator.

As illustrated in Figure 5.21, a bias current source is needed to provide the current for the ring oscillator stages. The output of the ring oscillator approximates a triangular wave with a voltage swing about 1.6 V as showing in Figure 5.22 (**ring_out**). A comparator is used to converter triangular wave to a square wave (**O_3** in Figure 5.23). As you can see from the plot, this square wave does not yield a 50% duty cycle. However, our PD can deal with square waves with arbitrary duty cycles. If an application asks for 50% duty cycle, a toggle flip flop can be added right after the comparator. This method is simple, but wastes half the frequency range. To synthesize kilohertz range frequencies, the bias currents glowing through transistors m_{bnn} and m_{bpp} in the range of 2-74 nA, while the oscillator frequency sweeps from 10-150 kHz. The

comparator current has been selected as 80nA to achieve sufficient speed. Since no extra load capacitor has been added to each stage output, the load capacitor of each stage is the input capacitor of the next stage. The input capacitor is the gate capacitor or the inverter pair and can be calculated using formula (5.11). If more accuracy is required, an additional term (the fringing capacitance) should be included to take into account the overlap between the gate and the source or drain area,

$$C_{gd} = C_{gs} \cong \frac{1}{2} WLC_{ox} + \underbrace{WL_{ov}C_{ox}}_{\text{fringing capacitance}} \qquad (5.11)$$

where: C_{ox} is gate oxide capacitance per unit area [5].

Table 5.2 lists the MOS transistor sizes for a single-ended 5-stage ring oscillator design. Since the electron mobility is 2-2.5 times higher than the holes mobility, we typically make the PMOS transistor 2 -2.5 times wider than the NMOS transistor to achieve similar rise and fall times. Figure 5.23 illustrates the expected linear relationship between frequency and power consumption. This single ended ring oscillator consumes 1 - 1.8μW over the entire frequency range.

Table 5.2. Dimension for transistors in single-ended ring oscillator (unit μm)

Inverter NMOS	**Inverter PMOS**	**mb_{pp}**	**mb_{nn}**	**mb_{p}**
1.2/12	2.4/12	4.8/1.2	4.8/1.2	4.8/1.2
mb_{n1}	**mb_{n2}**	**mb_{n3}**	**m_{cmp}**	**m_{cmn}**
4.8/1.2	4.8/1.2	4.8/1.2	2.4/12	1.2/12
mp_1	**mp_2**	**mp_3**	**mn_1**	**mn_2**
4.8/1.2	4.8/1.2	9.6/1.2	4.8/1.2	4.8/1.2

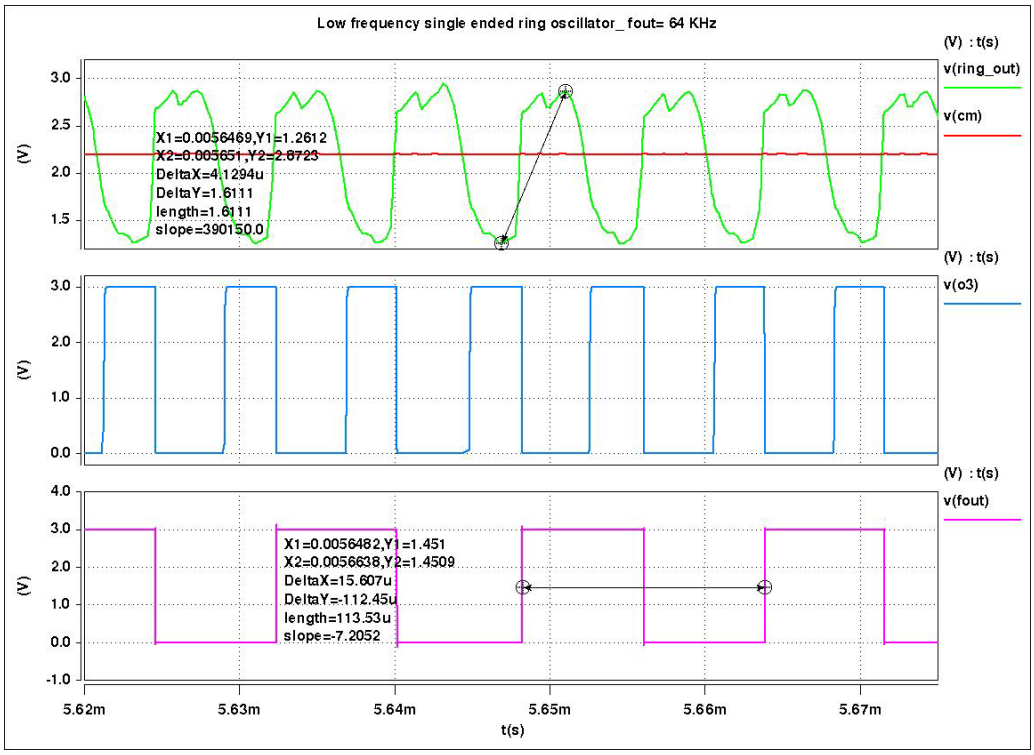

Figure 5.22. Simulation results for five-stage single ended ring oscillator (10-150 kHz).

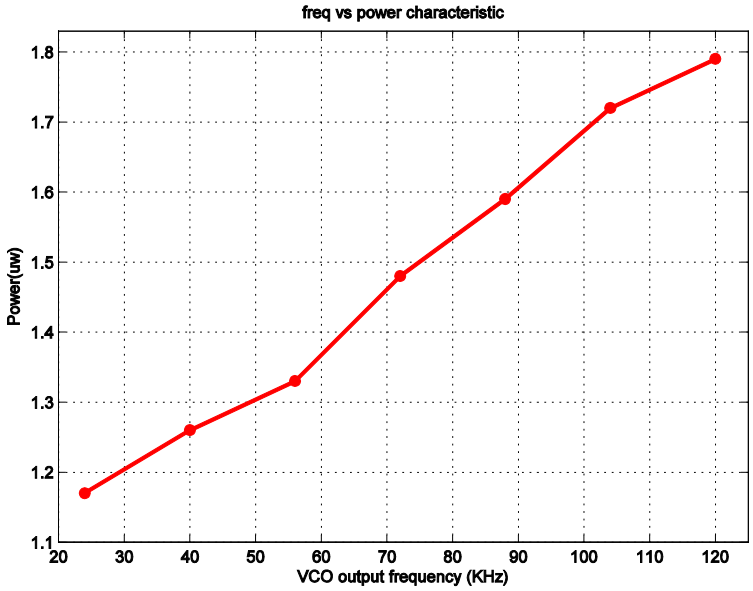

Figure 5.23. VCO output frequency with power dissipation.

B. Low speed differential ring oscillator (10- 150 kHz)

Fully differential ring oscillators have been used more often than single-ended oscillators, because of their good common mode reject ratio. Therefore, in the same power supply and substrate noise environment, fully differential ring oscillators yield less jitter caused by common mode noise. We have also implemented a five-stage differential ring oscillator which covers the same frequency range as the single-ended ring oscillator (10 - 150 kHz). Each stage is a current-controlled differential delay cell as shown in Figure 5.24.

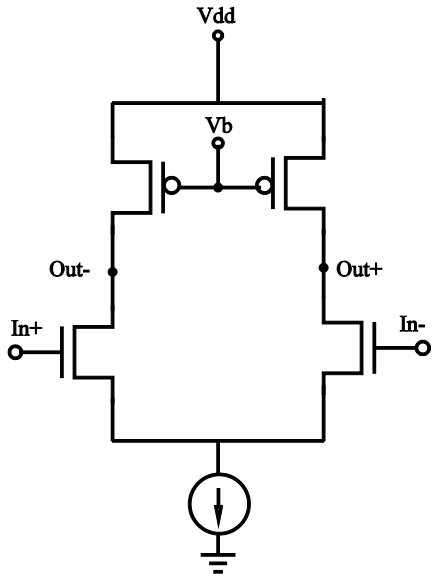

Figure 5.24. Differential delay element.

The delay cell is based on an NMOS source-coupled pair with a voltage controlled PMOS load pair. The tail current source is an NMOS transistor biased for maximum output swing. The delay cell is a function of the tail current I_{bias}, the differential voltage swing and the capacitance at out+ and out-. By controlling signal V_b to the PMOS pair, the voltage swing is held constant. If the capacitance is constant, then the delay T_d is inversely proportional to the variable bias current.

$$T_d = \frac{C_{tot} \cdot V_{swing}}{I_{bias}} \tag{5.12}$$

The dimensions for the PMOS and the NMOS pair in the delay cell are 2.4um/12um and NMOS are 1.2um/12um, respectively.

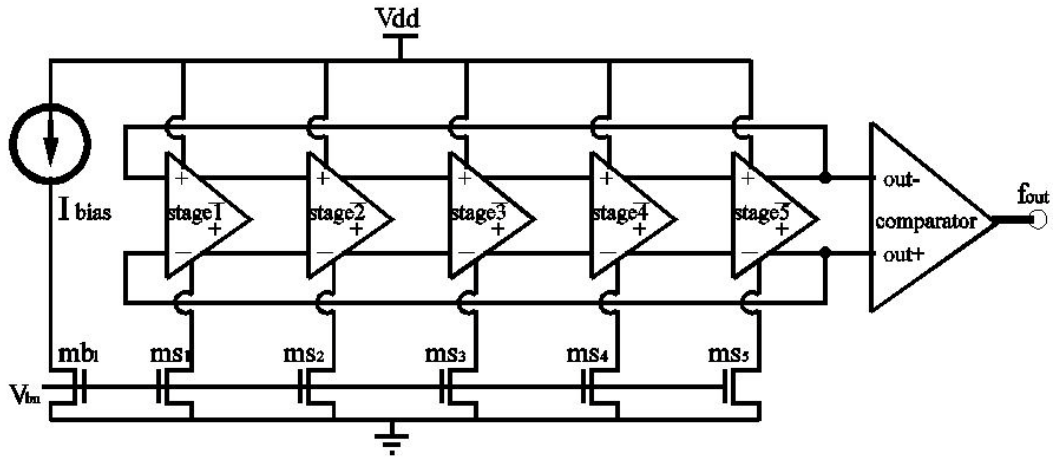

Figure 5.25. Five-stage differential ring oscillator.

The five-stage differential ring oscillator depicted in Figure 5.25 has 5 identical differential delay cell stages. Each stage is fully differential and the positive outputs are connected to the negative inputs of the next stage. The bias current is provided by a voltage to current generator that will be introduced in the next section. Transistors ms_1, ms_2, … ms_5 mirrored the currents into each stage. The output signals of the fifth stage are converted to the final VCO output (f_{out}) through a comparator. The comparator circuit is shown in Figure 5.26.

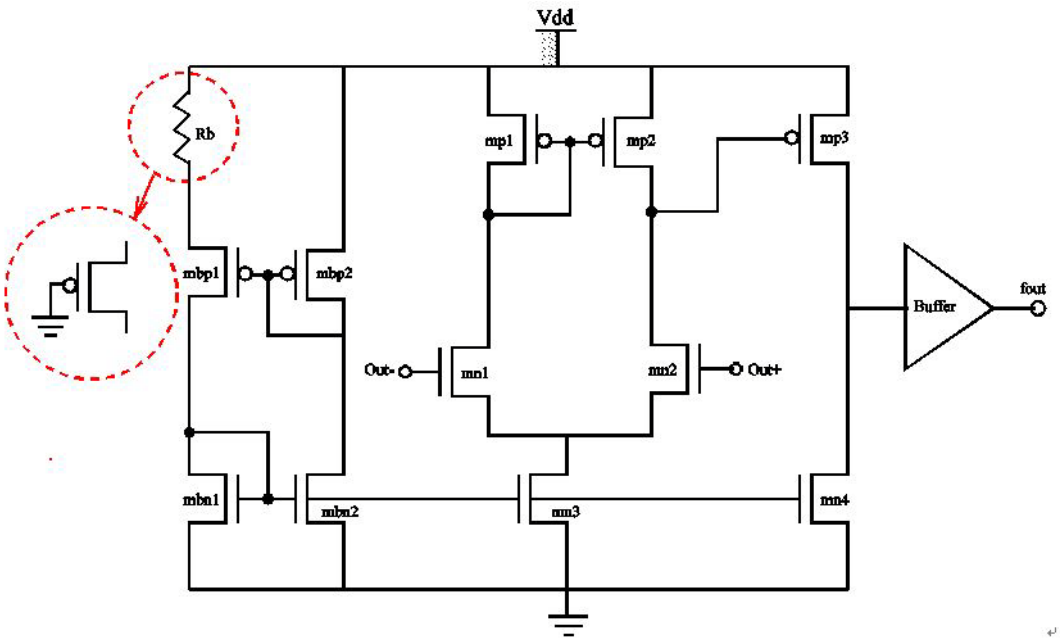

Figure 5.26. Comparator.

R_b can be implemented as a high-sheet-resistance polysilicon resistor or as a PMOS transistor. The linearity of this active resistor is a concern, but it does not impact the PLL jitter performance. As shown in equation (5.13), the active resistor is determined by the physical parameters μ_p, C_{ox}, W/L and V_{eff}.

$$R_{eq} = \frac{1}{\mu_p C_{ox}(\mathrm{W/L})\mathrm{V_{eff}}} \tag{5.13}$$

$$V_{eff} = V_{gs} - V_{tp} \tag{5.14}$$

where: μ_p is hole's mobility of PMOS. V_{tp} is PMOS threshold voltage.

Figure 5.27 presents the depicted buffer circuit to the comparator. It consists of a cascade of inverters. The factor xi underneath each inverter shows its relative size. The large output stage provides a shape clock signal nf_{out1}, since large inverters offer more current driving capability. nf_{out2}, f_{out} are fed to the digital counter of the PLL. f_{out} is considered the final output of the PLL .

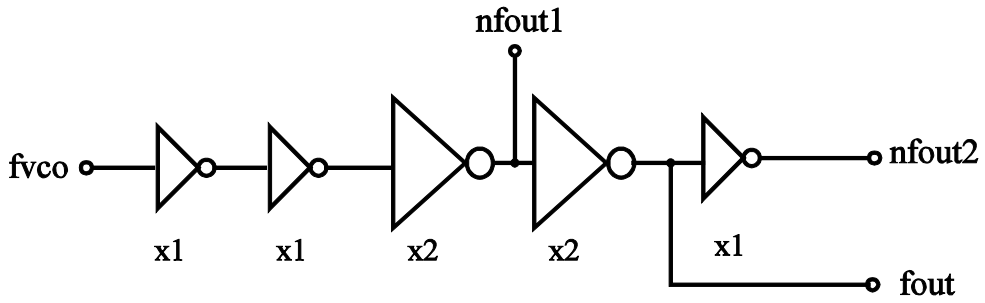

Figure 5.27. Buffer.

Table 5.3 lists all the sizes of transistors in comparator circuit.

Table 5.3. Dimension for transistors in comparator

$\mathbf{m_{bp1}}$	$\mathbf{m_{bp2}}$	$\mathbf{m_{bn1}}$	$\mathbf{m_{bn2}}$
6μm/1.2μm	4.8μm/1.2μm	3.6μm/1.2μm	3.6μm/1.2μm
$\mathbf{m_{p1}}$	$\mathbf{m_{p2}}$	$\mathbf{m_{n1}}$	$\mathbf{m_{n2}}$
6μm/1.2μm	6μm/1.2μm	6μm/1.2μm	6μm/1.2μm
$\mathbf{m_{p3}}$	$\mathbf{m_{n3}}$	$\mathbf{m_{n4}}$	$\mathbf{R_b}$
6μm*2/1.2μm	4.2μm/1.2μm	4.2μm/1.2μm	0.9μm/8.7μm

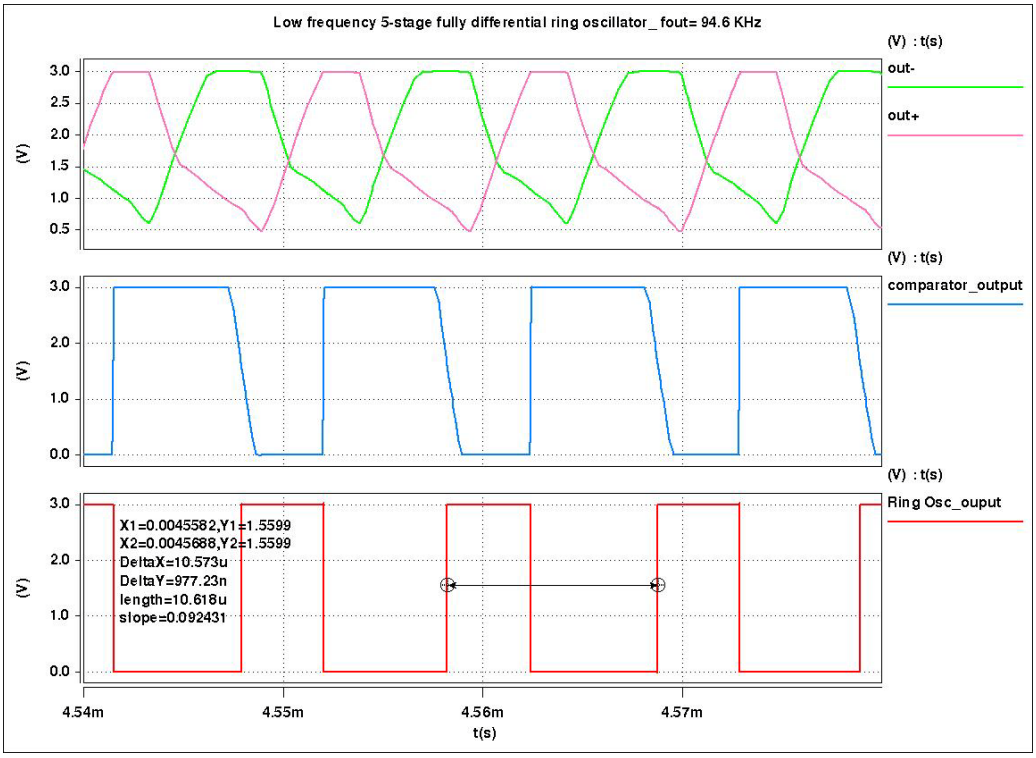

Figure 5.28 Simulation results for five-stage differential ring oscillator (10-150 kHz).

Figure 5.28 shows the HSPICE simulation results of this five-stage differential ring oscillator. out+ and out- are the outputs of the fifth stage of the ring oscillator. The swing is 2.5 V (0.5-3V). The comparator output is not a 50% duty cycle squarewave, since the pull-up speed is faster than the pull-down speed of our comparator. The delay cycle of the final ring oscillator output is therefore less than 50%. Recall that our phase detector circuit is insensitive to the duty cycle. So that the PLL still generates a constant frequency clock signal.

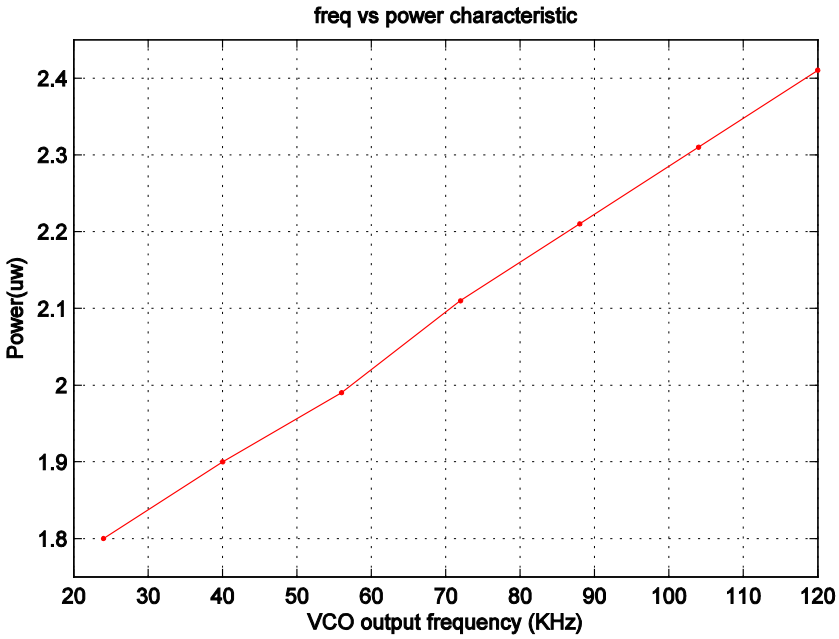

Figure 5.29. VCO output frequency versus power dissipation.

The power dissipation of the 5-stage differential oscillator is 1.8 - 2.4 μW over the frequency range. It consumes 0.6 μW more than the single-ended ring oscillator in Figure 5.23, since we increased the current of the comparator in the differential oscillator to improve the pull-up and pull-down capability. The ring stages of single-ended and differential oscillators consume a similar amount of power.

C. High frequency ring oscillator (10-100 MHz)

Fully differential ring oscillators are widely used and well suited for high speed applications. A five-stage high speed ring oscillator has also

been implemented, with a range of 10 -100 MHz. Since this frequency range is near the 0.5 μm standard CMOS technology speed limit, the layout required careful attention.

Based on equation (5.12), the most effective method to increase the frequency range is to raise the bias current. Recall that the low speed oscillator (10 - 150 kHz), utilized a bias current in the nA range. The high speed oscillator (10 -100 MHz), will require a bias current is in the μA range. The current change can be accomplished by modifying the voltage to current converter circuit as shown in section 5.4.

The high speed oscillator employs the same topology as illustrated in Figure 5.25. We slightly changed the device dimensions in each delay cell to better meet the high frequency operation. The bias current and the device sizes are listed in Table 5.4.

Table 5.4. Dimension for transistors in ring oscillator.

m_{bp1}(μm)	**m_{bp2}(μm)**	**m_{bn1}(μm)**	**m_{bn2}(μm)**
6/1.2	4.8/1.2	4.8/1.2	4.8/1.2
m_{p1}(μm)	**m_{p2}(μm)**	**m_{n1}(μm)**	**m_{n2}(μm)**
4.8/0.9	4.8/0.9	4.8/0.9	4.8/0.9
m_{p3}(μm)	**m_{n3}(μm)**	**m_{n4}(μm)**	**R_b(μm)**
4.8*2/1.2	4.8/1.2	4.8/1.2	1kΩ or 12/1.8
PMOS in delay element (μm)	**NMOS in delay element (μm)**	**Biased transistor (μm) in delay element (I_{bias})**	
4.8/1.2	3.6/0.9	4.8/1.2	

Table 5.5 lists comparator performances for high frequency fully differential ring oscillator.

Table 5.5. Comparator performance parameters

Circuit performance	Comparator
V_{dd} noise rejection	-6dB @10Meg @ 0.1mV Vdd noise, I_{bias}= 39uA
Gnd noise rejection	-21.3dB @ 10Meg @ 0.1mV Gnd noise, I_{bias}= 39uA
Differential mode gain	A_{dm}=53dB – 51dB from 280 kHz- 10 MHz
Common mode gain	A_{cm}=-3 – -5dB from 1MHz - 10 MHz

From Table 5.5., we shows that a better Gnd noise rejection than V_{dd} noise rejection. This high speed PLL is therefore more sensitivity to power supply noise than substrate noise.

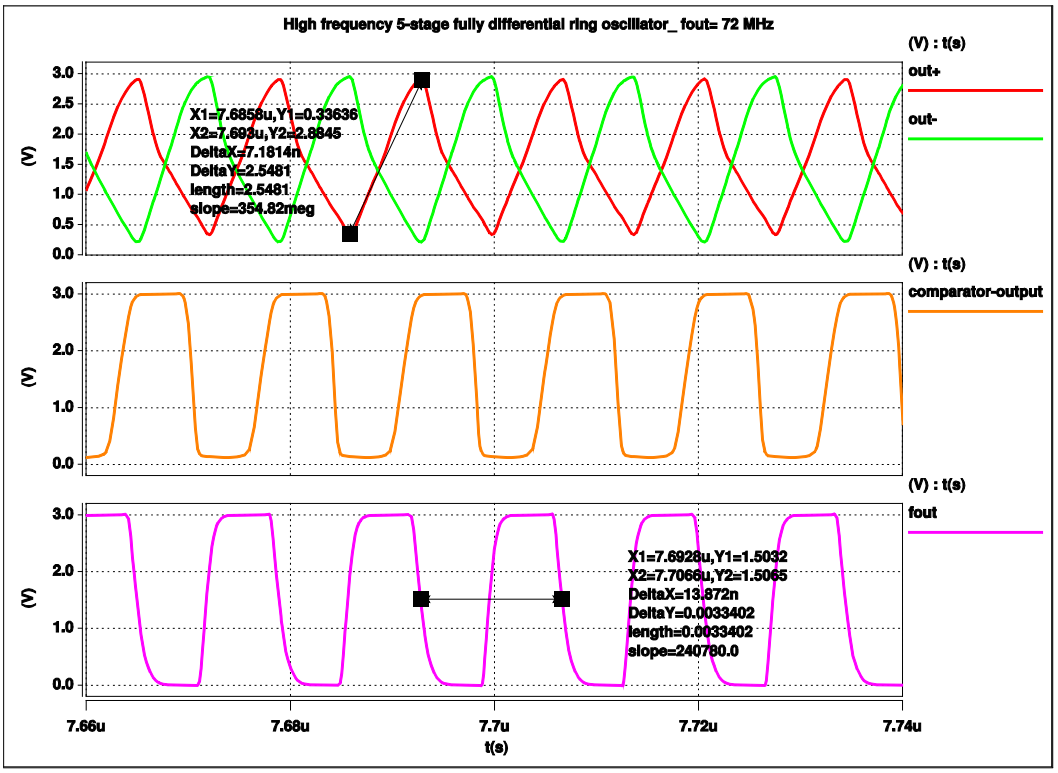

Figure 5.30. Simulation results for five-stage differential ring oscillator (10-100 MHz).

The swing of the outputs of the last delay stage (inputs to comparator) are 2.54 V. f_{out} illustrates a 72 MHz PLL output. Since the control voltage of the current converter circuit has been adopted for high speed, we carefully recorded the frequency characteristic as illustrated in Figure 5.31(a) and 5.31(b). This linear relationship reveals that the voltage to current converter yields a good voltage-current characteristic. The power consumption varies from 1.1 to 3.4mW over 10-100 MHz. This power range is nearly one thousand times higher than the range of the low speed (kHz) oscillator's.

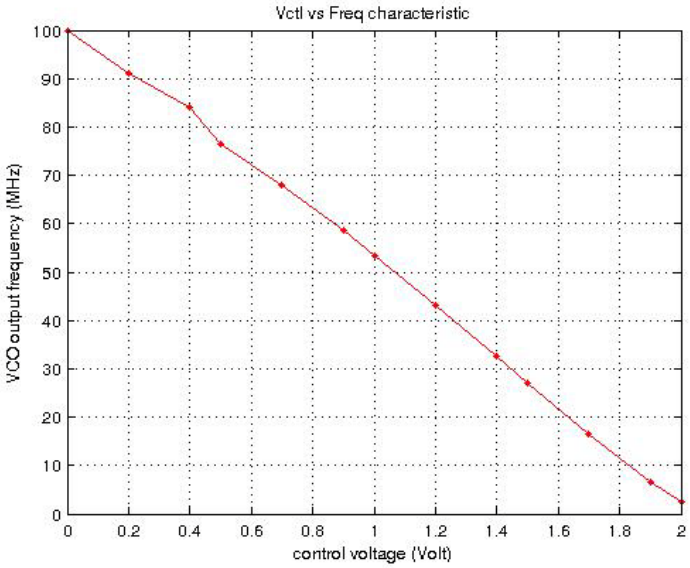

Figure 5.31(a). Control voltage versus output frequency.

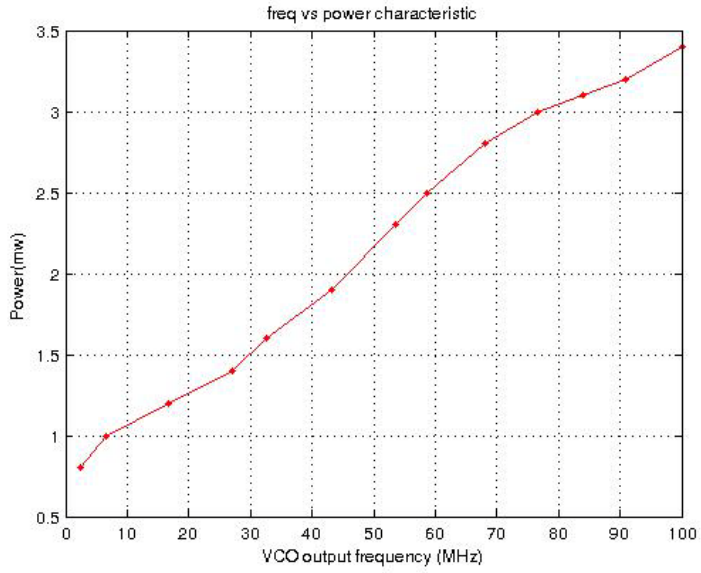

Figure 5.31(b). VCO output frequency versus power dissipation.

5.4 Voltage to current converter

Since the depicted relaxation and ring oscillators are all controlled by a bias current (I_{bias}), the charge pump output voltage needs to be converted to a proportional current. Unfortunately, the V-I relationship of an MOS device is not linear. To obtain a quasi-linear relationship, we have created a voltage dependent weighted sum of two nonlinear, very long channel MOS currents (the drain currents of mr1 and mr2 in Figure 5.32.) To avoid a dead-lock situation in case V_{ctl} accidently approaches V_{dd}, we have added a narrow start-up device mst, which prevents the control current I_{ctl} from reaching zero. The gate voltage V_b of the start-up device is approximately 2 V which is provided by another current source. Figure 5.33 shows a simulation of the resulting quasi-linear V-I curve realized by the depicted circuit intended for a low frequency range of (10 - 150 kHz). The drain currents of mr1 and m2 are not following a linear relationship, but the sum of the 2 currents a approximate linear voltage to current relationship. For MHz range applications, we simply have to adjust the W/L ratios of mr1 and mr2. This reduces the equivalent resistance (eq. 5.13) and thus increased the current. The quasi-linear voltage to current relationship is therefore preserved. The transistor dimensions in the

voltage to current converter are listed as in Table 5.6. This simple design not only saves die area and complexity, but also provides the flexibility to convert low speed PLL to high speed PLL.

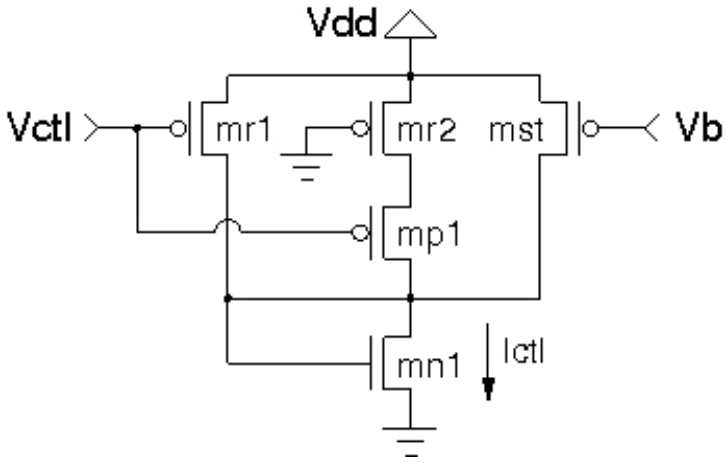

Figure 5.32. Voltage-to-current converter circuit.

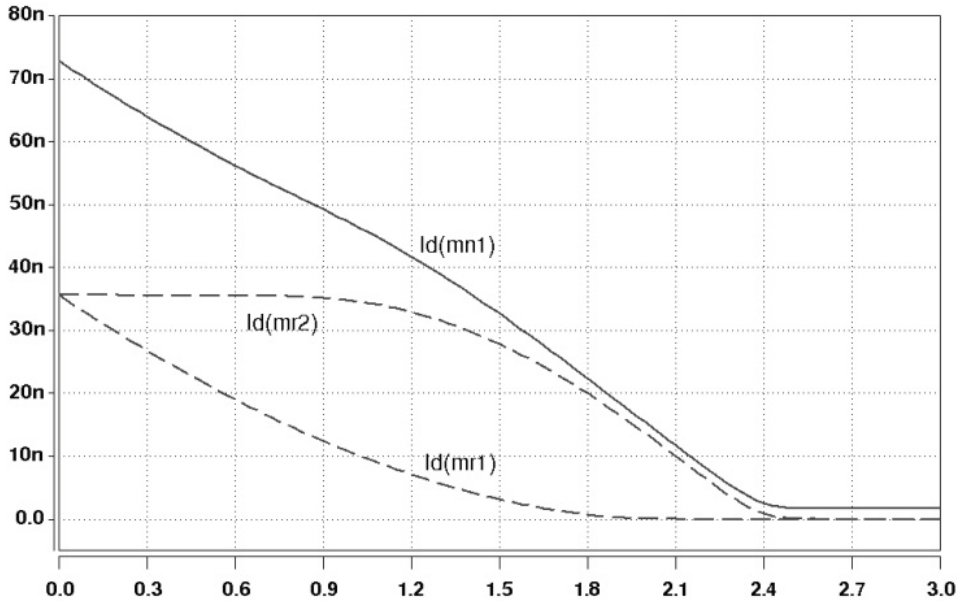

Figure 5.33. Resulting V-I Converter Characteristics.

Table 5.6. The dimension of transistors in V-I converter

	mr1(μm)	**mr2(μm)**	**mp1(μm)**	**Mst(μm)**
Low frequency VCO	0.9/360	0.9/360	6/0.6	0.9/1.5
High frequency VCO	1.8/0.6	1.8/0.6	6/0.6	0.9/1.5

5.5 Divide by N circuit

5.5.1 Normal divide by N logic

The utilization of a divide-by-N or modulo N counter renders the PLL more versatile. By combining the divider circuit with a digital comparator, one effectively has a frequency synthesizer governed by the simple relationship.

$$f_{out} = N \cdot f_{in} \tag{5.15}$$

If it becomes necessary to create fractional multiples of a reference frequency, one can add a second divide-by-M circuit in front of the PD. The complete PLL diagram is depicted in Figure 5.34. The output versus input frequency relationship then becomes:

$$f_{out} = \frac{N}{M} \cdot f_{in} \tag{5.16}$$

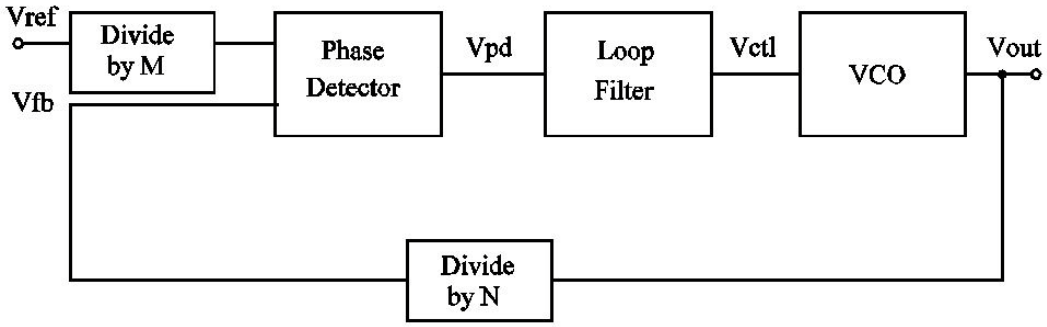

Figure 5.34. Frequency synthesizer with f_{out} = fractional multiple of reference frequency.

We have applied this technique to synthesize output frequencies of integer multiples of ¼ of the typical watch crystal frequency of 32.756 kHz. Figure 5.35 depicts our 4-bit version of a divide-by-N counter paired with the necessary digital comparator circuit. This circuit enables testing the PLL for any integer number of N between 1 and 15. The divider and comparator circuits have been implemented using static CMOS techniques. Since this counter/comparator circuit is operated at frequencies below 125 kHz, its contribution to the total power budget is deemed negligible.

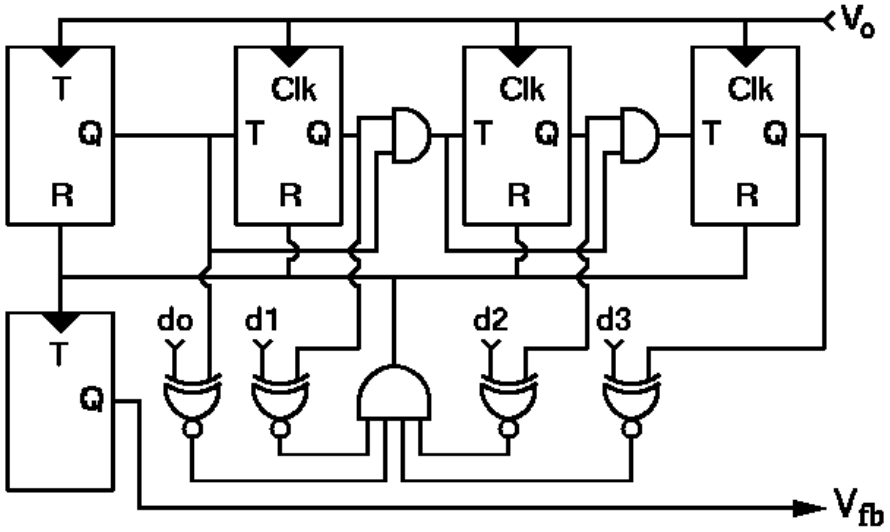

Figure 5.35. Divide by N counter for low frequency PLL (10-150 kHz).

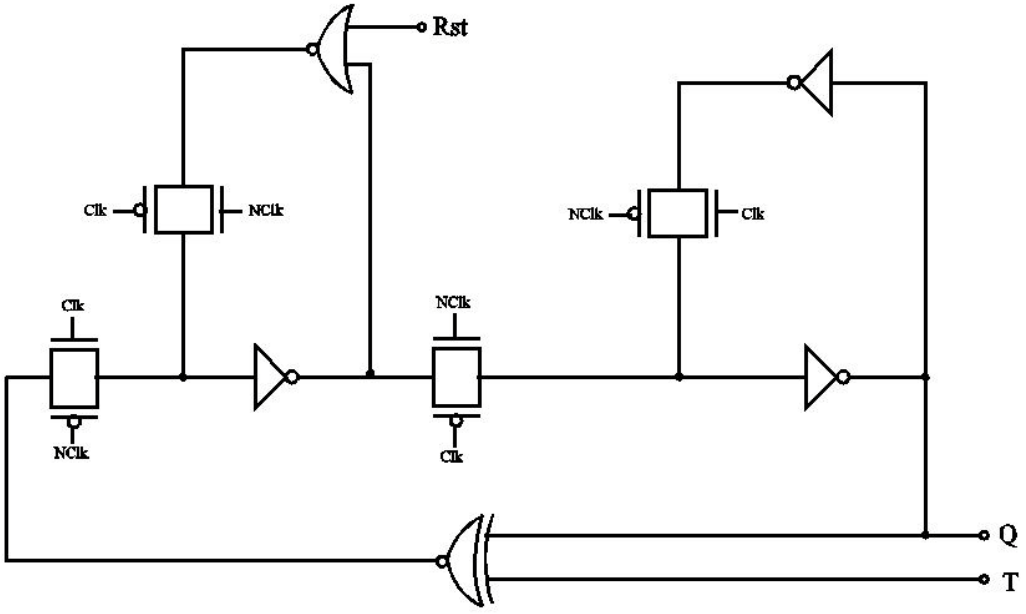

Figure 5.36. TFF in Divide by N counter.

5.5.2 Divide by N+1 counter

The reset signal of the preserved divide by N counter only lasts for several nano seconds. This is safe for the low frequency (kHz) range operation. For high frequency applications, we have utilized a more noise immune design by replacing the Divide by N counter in Figure 5.35 with a Divide by N+1 counter as shown in Figure 5.37. This provides a well defined reset time of half clock for all TFFs. The output versus input frequency relationship then becomes:

$$f_{out} = (N+1) \cdot f_{in} \tag{5.17}$$

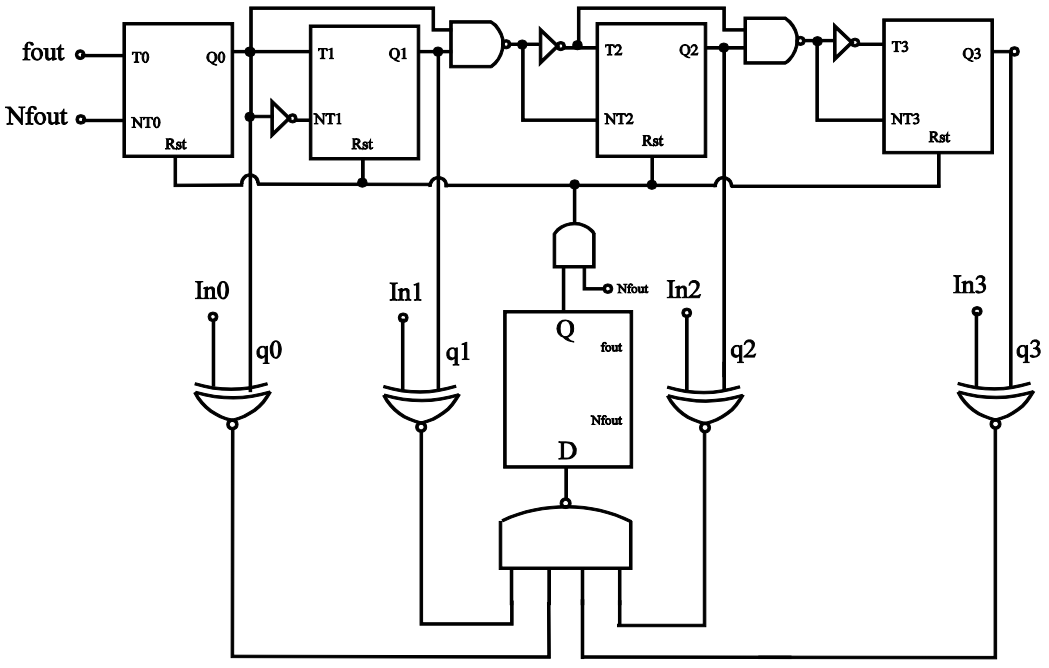

Figure 5.37. Divide by N+1 counter for high frequency PLL (10-100 MHz).

References:

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[5] "Digital Integrated Circuit Design", Ken Martin, 1999.

Chapter 6

Jitter analysis and PLL model

6.1 PLL jitter analysis

As represented in Figure 5.7, a PLL comprises four basic building blocks (phase discriminator，charge pump, VCO, digital counter). Technically, they all generate noise and contribute to phase jitter. However, the VCO and the CP are the strongest contributors to the jitter performance. Consequently, we approximately equate the VCO phase noise to the phase noise of the PLL output. This section addresses the jitter analysis of a relaxation oscillator and a differential ring oscillator in 6.1.1 and 6.1.2, respectively.

6.1.1 Jitter analysis of relaxation oscillator

If a PLL operates in the locked state, the output voltage of the filter, in our case the charge-pump, should remain constant. Consequently, the (ternary) phase discriminator (PD) and the charge pump (CP) are in a quasi standby state, since neither block actively contributes to the operation of the VCO. Practically, the phase discriminator is affected

by jitter on both of its inputs, i.e., the reference frequency and the digital counter output (feedback signal). If the voltage spikes created by the PD output are sufficiently long, they will impact the charge pump and in turn the VCO control voltage $\mathbf{V_{ctl}}$. Albeit not expected to be significant, we will represent the collective impact of the PD and the charge pump in our analysis by an equivalent noise voltage $\mathbf{V_{nctl}}$.

A. Noise analysis in VCO

A full period of the VCO output waveform comprises two periods of the sawtooth voltage V_r (cf. Figure 5.16 in Chapter 5). If we assume that the variations between two adjacent periods of V_r are statistically independent, we can write the standard deviation of the VCO period jitter as

$$\sigma_{VCO} = \sqrt{2}\sigma_{saw} \tag{6.1}$$

where σ_{saw} denotes the variance or jitter of the sawtooth. As illustrated in Figure 6.1, the period jitter σ_{saw} of the sawtooth wave stems from two distinct sources. The first source is noise residing on the two rail voltages V_{dd} and V_{ref}. The second source is noise riding on top of the constant ramp current I_r (cf. Figure 5.13 or 5.14 in Chapter 5). Note that a very similar argument can be applied to a ring oscillator

circuit. In the latter case, the sawtooth has to be replaced by a triangular wave, which mimics the rising and falling outputs of the cascaded inverters or differential gain stages forming the oscillator.

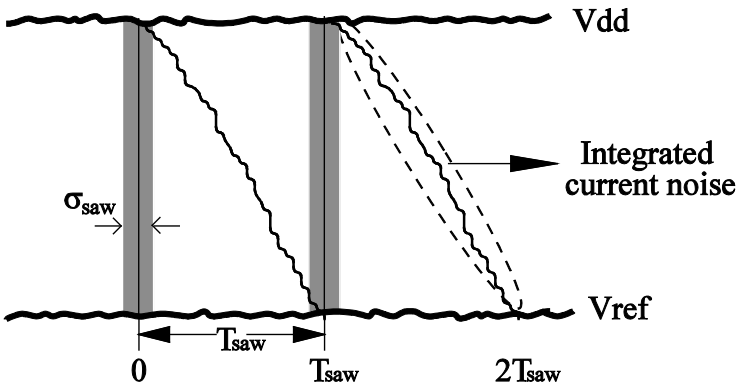


Figure 6.1. Noise and period jitter of sawtooth wave.

If we summarize the disturbances stemming from the two rail voltages by an equivalent noise voltage V_n, we can express the corresponding variation of the sawtooth period as

$$\sigma_{saw_V} = \frac{V_n T_{saw}}{V_{dd} - V_{ref}} \tag{6.2}$$

The contribution of the current noise can be written as

$$\sigma_{saw_I} = \frac{T_{saw}}{(V_{dd} - V_{ref})C_r} \int_0^T I_n dt = \frac{1}{I_r} \int_0^T I_n dt \tag{6.3}$$

We presume that variations of the rail voltages are primarily caused by

locally injected noise. The current noise, on the other hand, mostly stems from the MOS devices of the ramp current generator (cf. Figure 6.2). We therefore consider the two noise sources to be very weakly correlated. The variation of the sawtooth period can then be approximate by

$$\sigma_{saw} = \sqrt{\sigma_{saw_V}^2 + \sigma_{saw_I}^2} \tag{6.4}$$

By modeling the current noise I_n as a finite sum of small sinusoids, we can rewrite the integrated current noise as

$$\int_0^T I_n dt = T \sum_k I_k \underbrace{\frac{\sin(\omega_k T + \varphi_k) - \sin(\varphi_k)}{T\omega_k}}_{F_k} \tag{6.5}$$

The function F_k in the above equation acts similar to a lowpass filter, more specifically a sin(x)/x function, which progressively attenuates the amplitude of component I_k as ω_k increases. We can therefore replace F_k by a unity-gain brick wall filter of equivalent bandwidth $B_{EQ}=0.5f_{vco}$. Due to the short sawtooth reset time, the integrating time T is essentially equal to T_{saw}. Finally, we can replace I_n by the effective spectral noise current density I_{fn}. This yields the following approximation for the integrated current:

$$\int_0^{T_{saw}} I_n dt \approx T_{saw} \cdot I_{fn} \sqrt{0.50 f_{vco}} \qquad (6.6)$$

and leads to the following approximation for the sawtooth jitter

$$\sigma_{saw} \approx T_{saw} \sqrt{\frac{V_n^2}{(V_{dd} - V_{ref})^2} + \frac{I_{fn}^2 f_{vco}}{2 I_r^2}} \qquad (6.7)$$

B. Noise analysis in PD and loop filter

As previously mentioned, the loop filter only contributes significant switching noise while the PLL is in transition. Once the frequency is locked, the control voltage remains essentially constant. The only significant disturbance on the VCO input V_{ctl} is noise injected from the supply rails. This input noise source is represented by V^2_{nctl} in Figure 6.2. Its main contribution will be an additional independent noise current component I^2_{ctln} generated by transistor mr1 as shown in equation 6.8.

C. Simulated current noise power and VCO relative jitter

Figure 6.2 depicts the voltage-to-current converter with all noise sources we considered in our noise analysis.

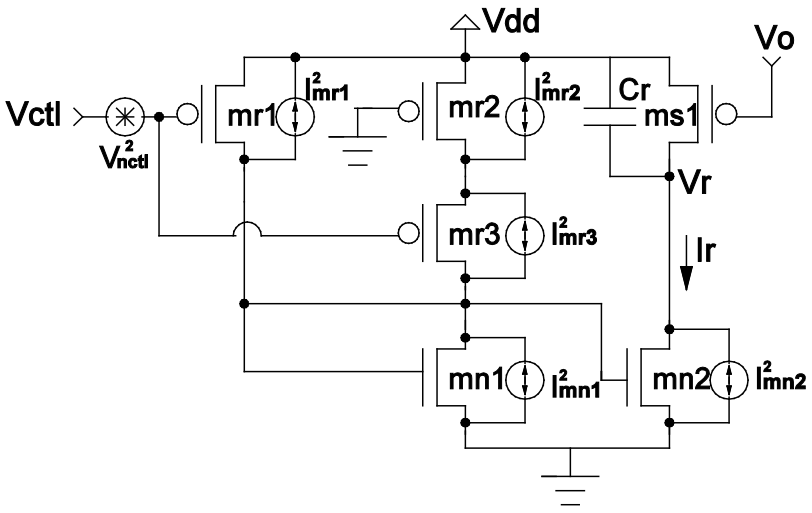


Figure 6.2. V-I converter and noise sources.

To obtain a quasi-linear relationship between control voltage and ramp current, we have summed up the two nonlinear drain currents of the long channel transistors mr1 and mr2, respectively. Note that transistor mr1 operates in saturation while mr2 works in the triode region. The short channel devices mr3, mn1 and mn2 are biased in the sub-threshold region. The contributions of mr1 and mr2 are predominantly of thermal nature, while mr3, mn1 and mn2 primarily add shot noise described by the equivalent current density $2qI_d$. Transistor ms1 serves to reset the sawtooth voltage and thus does not significantly contribute to the total current noise. Since the VCO is operating over a comparatively low frequency range, flicker noise should be considered as well. However, a preliminary numerical

analysis of low frequency noise carried out using the McWhorter model [3] has revealed that this contribution is relatively insignificant when compared to thermal and sub-threshold shot noise. The total current noise power I^2_{fn} can therefore be approximated by the sum of the total transistor current noise power I^2_{dn} and the noise power I^2_{ctln} caused by V^2_{nctl} at the gate of mr1.

Table 6.1 Transistor internal current noise power in different operation regions

	I^2_d	Noise type
Triode region	$4KT(2/3)g_m$	Thermal noise
Saturation region	$4KTg_{ds}$	Thermal noise
Sub-threshold region	$2qI_d$	Shot noise

Then, the total current noise power I^2_{fn} becomes:

$$I_{fn}^2 = I_{dn}^2 + I_{ctln}^2 \tag{6.8}$$

$$I_{ctln}^2 = \mathrm{I}_{mr1}^2 = \mathrm{V}_{\mathrm{nctl}}^2 \cdot g_{m\,mr1}^2 \tag{6.9}$$

$$I_{dn}^2 = 4kT(\frac{2}{3}\mathrm{g_{m\,mr1}} + g_{ds\,\mathrm{mr2}}) + 2q(\mathrm{I_{d\,mr3}} + \mathrm{I_{d\,mn1}} + \mathrm{I_{d\,mn2}}) \qquad (6.10)$$

The internal transistor current noise power is listed in Table 6.1. Since jitter scales as the VCO frequency, it is more practical to compare the performance on a relative basis by dividing the jitter by the period of the output frequency. The resulting relative jitter at the VCO output can be written as

$$J_{vco} = \frac{\sigma_{vco}}{T_{vco}} \approx \sqrt{\frac{V_n^2}{2 \cdot V_{swing}^2} + \frac{f_{vco}}{4}(\frac{I_{fn}}{I_{bias}})^2}$$

$$\approx \sqrt{\underbrace{\frac{V_n^2}{2(V_{dd} - V_{ref})^2}}_{\mathrm{J_1^2}} + \underbrace{\frac{I_{dn}^2 f_{vco}}{4I_r^2}}_{\mathrm{J_2^2}} + \underbrace{\frac{V_{nctl}^2 g_{m(\mathrm{mr1})}^2 f_{vco}}{4I_r^2}}_{\mathrm{J_3^2}}} \qquad (6.11)$$

The J^2_1 term in the above equation represents jitter induced by rail voltage noise, while J^2_2 and J^2_3 represent contributions stemming from the integrated ramp current noise caused by the MOS transistors and the equivalent noise on the control voltage V_{ctl}, respectively. Table 6.2 lists the equivalent jitter components J_1 and J_3 as a single sum, since we cannot analytically differentiate between the two sources. The values for J_2 are based on the simulated device current values of VCO1 (relaxation oscillator with 2.4 V swing).

Table 6.2 Jitter contribution versus output frequency

N	F_{ref} [kHz]	F_{out} [kHz]	J_1+J_3 Jitter [%]	J_2 Jitter [%]	Measured Jitter J_{vco} [%]
4	8.192	32.768	0.1264	0.0660	0.143
6	8.192	49.152	0.0932	0.0644	0.113
8	8.192	65.536	0.0887	0.0629	0.109
10	8.192	81.920	0.0848	0.0603	0.104
12	8.192	98.304	0.0986	0.0589	0.115
14	8.192	114.688	0.1095	0.0558	0.123

The current noise induced jitter component shows a weak inverse dependence on the ramp current I_r. The J_2 contribution will therefore become progressively smaller as the PLL frequency increases. Consequently, jitter in high-frequency PLLs is expected to be dominated by (injected) voltage noise rather than device current noise. Our measurements revealed that the J^2_2 term shrinks from 4.36×10^{-7} to 3.11×10^{-7} as the frequency increases from 32.768 kHz to 114.688 kHz. This corresponds to relative jitter values of 0.066% and 0.0558 % at the lower and upper frequency range, respectively. The computed J_2 values account for approximately half of the observed jitter. The

current induced jitter can therefore serve as a realistic lower bound in the investigated ultra-low power low frequency PLLs.

6.1.2 Jitter analysis of differential ring oscillator

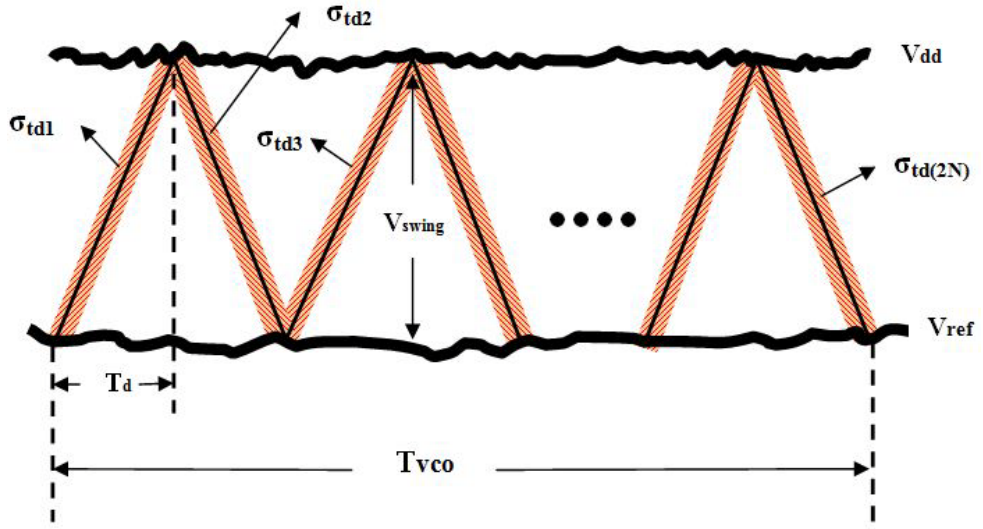


Figure 6.3. Noise and period jitter on rise and fall time for each ring stage.

If the ring oscillator has N stages, the period of its output is

$$T_{vco} = 2 \cdot N \cdot T_d = \frac{2 \cdot N \cdot C_{tot} \cdot V_{swing}}{I_{bias}} \tag{6.12}$$

$$I_{bias} = \frac{2 \cdot N \cdot C_{tot} \cdot V_{swing}}{T_{vco}} \tag{6.13}$$

For each stage, the rising and falling edges have the same delay time T_d. The time jitter of T_d is defined as σ_{td} as revealed in Figure 6.3.

Practically, the output transitions are delayed by the latency of the comparator. If we neglect this latency, as depicted in Figure 6.3, the jitter observed at the VCO output is caused by the jitter of each T_d. We denote the fuzziness (noise) riding on rising edge delay by σ_{td1} while σ_{td2} represents noise on the falling edge delay. The variation of the VCO output σ_{vco} is a synthesis of time jitter on each delay.

A full period of the N stage ring oscillator output waveform comprises 2N delays as stated in (6.12). If we assume the noise on each delay to be equal,

$$\sigma_{td1} = \sigma_{td2} = \sigma_{td3} = \cdots = \sigma_{td(2N)} = \sigma_{td} \qquad (6.14)$$

and the variations between any two adjacent delays to be statistically independent, we can write the standard deviation of the VCO period jitter as

$$\sigma_{vco} = \sqrt{\sigma_{td1}^2 + \sigma_{td2}^2 + \cdots + \sigma_{td(2N)}^2} = \sqrt{2N} \cdot \sigma_{td} \qquad (6.15)$$

In what follows, we will discuss the relationship between delay time jitter and relative VCO jitter. The analysis will consider power rail

noise and integrated current noise.

We define the swing voltage $V_{swing}=V_{dd}-V_{ref}$ as presented in Figure 6.3 and we presume that the variations of the swing voltages are primarily caused by locally injected noise or power rail noise. We defined that the variation of T_d caused by power rail noise is σ_{td_v}. The current noise, on the other hand, mostly stems from the MOS devices of the ramp current generator. σ_{td_I} represents the variations caused by current noise. We therefore consider the two noise sources to be very weakly correlated. The variation of the T_d can then be approximate by

$$\sigma_{td}=\sqrt{\sigma_{td_V}^2+\sigma_{td_I}^2} \tag{6.16}$$

$$\sigma_{td_V}=\frac{V_n}{V_{swing}}\cdot T_d \tag{6.17}$$

$$\sigma_{td_I}=\frac{1}{I_{bias}}\int_0^{T_d} I_n dt \tag{6.18}$$

By modeling the current noise I_n as a finite sum of small sinusoids,

$$I_n=\sum_k I_k\cos(\omega_k t+\varphi_k) \tag{6.19}$$

we can rewrite the integrated current noise as (6.5). The function F_k in equation 6.5 acts similar to a lowpass filter, more specifically a sin(x)/x function, which progressively attenuates the amplitude of component I_k as ω_k increases.

$$F_k \approx \frac{\sin(\omega_k T)}{\omega_k T} = H(\omega) \tag{6.20}$$

We can therefore replace F_k by a unity-gain brick wall filter of equivalent bandwidth B_{EQ}.

$$B_{EQ} = \int_0^\infty \left|H(\omega)\right|^2 df \tag{6.21}$$

$$B_{EQ} = \int_0^\infty \frac{(\sin 2\pi ft)^2}{2\pi ft^2} df = \frac{1}{2\pi T}\int_0^\infty \frac{\sin x^2}{x^2} dx = \frac{1}{4T} \tag{6.22}$$

For ring oscillator, T is the delay time T_d.

$$T = T_d = \frac{1}{2N} \cdot f_{vco} \tag{6.23}$$

Then, the equivalent bandwidth of F_k is

$$B_{EQ} = \frac{1}{4 \cdot \frac{1}{2N} \cdot T_{vco}} = \frac{N}{2} \cdot f_{vco} \tag{6.24}$$

Thus, the total current noise is the product of current noise density and the square root of equivalent bandwidth B_{EQ}.

$$I_n = I_{fn}\sqrt{B_{EQ}} = I_{fn}\sqrt{\frac{N}{2}\cdot f_{vco}} \tag{6.25}$$

The integrated current noise on T_d can be presented as

$$\sigma_{td_I} = \frac{1}{I_{bias}}\int_0^{T_d} I_n dt = \frac{I_{fn}}{I_{bias}}\cdot T_d \cdot \sqrt{\frac{N}{2}\cdot f_{vco}} \tag{6.26}$$

Utilizing equations 6.16, 6.17 and 6.26 yields 6.27 and the jitter of T_d can be described as

$$\sigma_{td} = T_d\sqrt{\frac{V_n^2}{V_{swing}^2} + \frac{I_{fn}^2}{I_{bias}^2}\cdot\frac{N}{2}\cdot f_{vco}} \tag{6.27}$$

Utilizing equations 6.12, 6.15 and 6.27 yields 6.28 and the relative period jitter of VCO output is

$$\begin{aligned} J_{vco} = \frac{\sigma_{vco}}{T_{vco}} = \frac{\sqrt{2N}\sigma_{td}}{2N\cdot T_d} &\approx \frac{1}{\sqrt{2N}}\cdot\sqrt{\frac{V_n^2}{V_{swing}^2} + \left(\frac{I_{fn}}{I_{bias}}\right)^2\cdot\frac{N}{2}\cdot f_{vco}} \\ &= \sqrt{\frac{1}{2N}\cdot\frac{V_n^2}{V_{swing}^2} + \frac{1}{4}\cdot\frac{I_{fn}^2}{I_{bias}^2}\cdot f_{vco}} \end{aligned} \tag{6.28}$$

As mentioned in 6.1.1, we will include the contribution of the CP in our analysis by an equivalent noise voltage V_{nctl}. This voltage can be viewed as an extra noise source added to the current generator input, i.e. the gate of mr1. Transistor mr1 in Figure 6.2 converts the voltage noise to current noise (I^2_{ctln}), which becomes part of the current noise power of the VCO. The total current noise power I^2_{fn} can therefore be approximated by the sum of the total transistor current noise power I^2_{dn} and the noise power I^2_{ctln} caused by V^2_{nctl} at the gate of mr1. Then, the total current noise power I_{fn}^2 and the relative jitter for the differential ring oscillator can be written as

$$I_{fn}^2 = I_{dn}^2 + I_{ctln}^2 = I_{dn}^2 + V_{nctl}^2 g_{m(mr1)}^2 \tag{6.29}$$

$$J_{vco} = \frac{\sigma_{vco}}{T_{vco}} = \sqrt{\underbrace{\frac{V_n^2}{2N \cdot V_{swing}^2}}_{J_1^2} + \underbrace{\frac{f_{vco}}{4}\left(\frac{I_{dn}}{I_{bias}}\right)^2}_{J_2^2} + \underbrace{\frac{f_{vco}}{4}\left(\frac{V_{nctl} g_{m(mr1)}}{I_{bias}}\right)^2}_{J_3^2}} \tag{6.30}$$

Since we use the same ramp current generator to provide current, the equation for I^2_{dn} in section 6.1.1 can be applied here as well.

$$I_{dn}^2 = 4kT\left(\frac{2}{3}\mathrm{g_{mmr1}} + g_{ds\,\mathrm{mr2}}\right) + 2q(\mathrm{I_{dmr3}} + \mathrm{I_{dmn1}} + \mathrm{I_{dmn2}}) \tag{6.31}$$

Note that the jitter of the ring oscillator caused by power rail noise can be reduced by increasing N. However, the oscillator consumes more power with larger N. Consequently, the choice of the number of stages is compromising between accuracy and power dissipation. Moreover, the expression of the jitter caused by integrated current noise of ring (eq. 6.28) and relaxation oscillator (eq. 6.11) are the same.

The previous analysis investigated the noise sources found in relaxation and differential ring oscillators. The current noise term J_2^2 in (6.30) has been considered as a suggested predictor. It is easier to be estimated for simulation purposes than supply and substrate noise and can serve as a lower bound for jitter.

6.2 PLL model

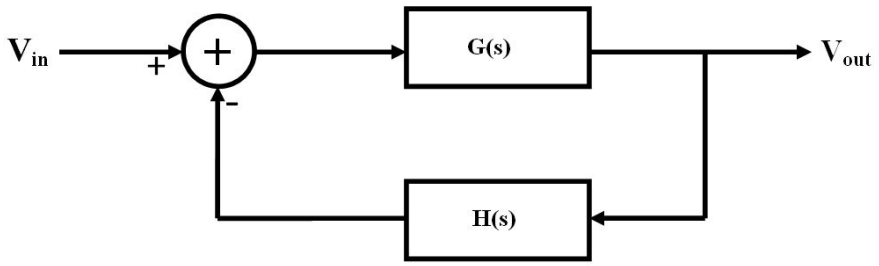


Figure 6.4 Basic feedback network of PLL

Figure 6.4 is a diagram of a basic feedback network with transfer

function.

$$\widetilde{H}(s) = \frac{\mathrm{G(s)}}{1 + \mathrm{H(s)G(s)}} \tag{6.32}$$

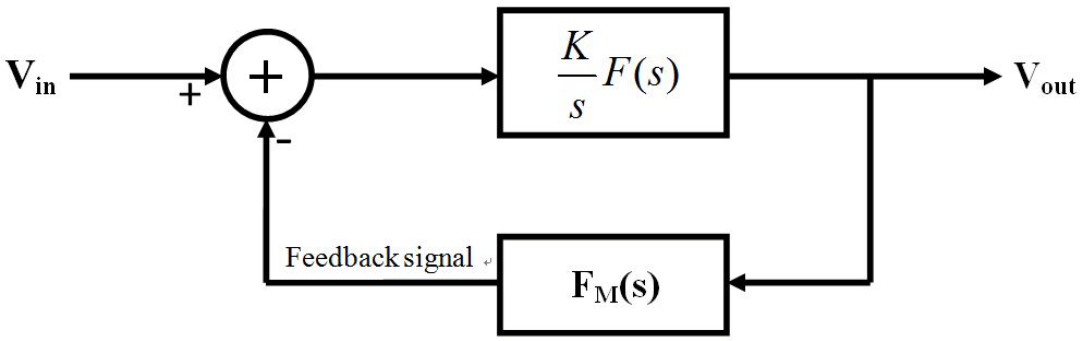


Figure 6.5. Basic feedback network of PLL.

As shown in Figure 6.5, the PLL is a feedback system, with

$$G(\mathrm{s}) = \frac{\mathrm{K}}{\mathrm{s}} F(s) \tag{6.33}$$

$$H(\mathrm{s}) = F_M(s) \tag{6.34}$$

The transfer function of the PLL can be written as

$$H_{PLL}(\mathrm{s}) = \frac{\frac{K}{s}F(s)}{1 + F_M(s)\frac{K}{s}F(s)} = \frac{KF(s)}{s + F_M(s)\cdot K \cdot F(s)} \tag{6.35}$$

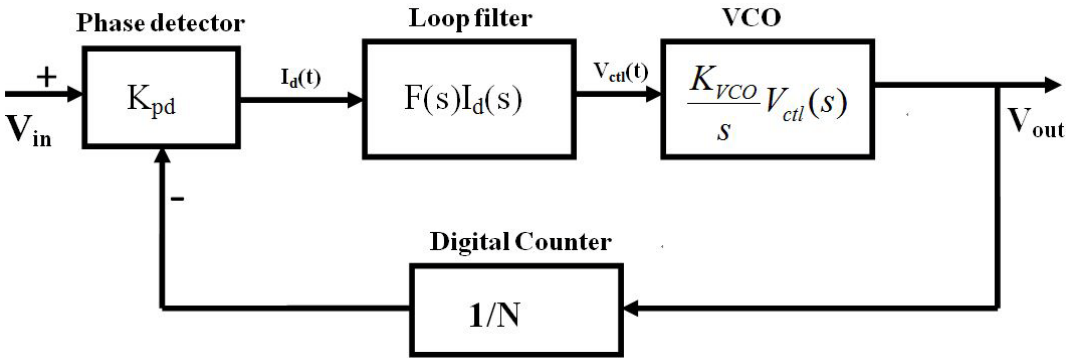


Figure 6.6. PLL diagram with modeling of each block.

Figure 6.6 illustrates the modeling of each functional block [1] [2]. K_{pd} is called phase detector gain and K_{vco} is the VCO gain. The K factor in Figure 6.5 is

$$K = K_{pd}K_{VCO} \tag{6.36}$$

High VCO gain will provide a large oscillator bandwidth, but the PLL will be more sensitive to noise. Low VCO gain will render the system immune to interference at the cost of a diminished frequency range. Hence, the selection of the VCO gain is a compromise between jitter performance and frequency range. The F(s) factor of the loop filter block in Figure 6.6 presents the transfer function of charge pump (cf. equation 5.1 in Chapter 5).

$$F(\mathrm{s}) = \frac{1 + \mathrm{RC}_1 S}{C_1 S} \tag{6.37}$$

Where $F_M(s)$ is a feedback factor, which normally depends on a digital

counter in the feedback path. The scalar N characterizes the frequency divider.

$$F_M(\mathrm{s}) = \frac{1}{\mathrm{N}} \tag{6.38}$$

By substituting equations (6.36) (6.37) (6.38) into (6.35), one can approximate the transfer function of a PLL employing a charge pump by:

$$\begin{aligned} H_{PLL}(\mathrm{s}) &= \frac{K_{VCO}K_{pd}\dfrac{1+RC_1 s}{C_1 s}}{s + K_{VCO}K_{pd}\dfrac{1+RC_1 s}{C_1 s}\cdot\dfrac{1}{N}} \\ &= \frac{K_{VCO}K_{pd}(\dfrac{1}{C_1}+sR)}{s^2 + s\dfrac{1}{N}K_{pd}K_{VCO}R + \dfrac{K_{pd}K_{VCO}}{NC_1}} \end{aligned} \tag{6.39}$$

where $$K_{pd} = \frac{I_{ch}}{2\pi} \tag{6.40}$$

and $$K_{vco} = \frac{\Delta\omega}{\Delta V_{ctl}} \tag{6.41}$$

K_{pd} and K_{vco} have units of Amp/rad and Hz/V, respectively, while I_{ch} is the charge pump current. $\Delta\omega$ is the VCO operating frequency range and ΔV_{ctl} is the variation of the control voltage corresponding to $\Delta\omega$.

The PLL's natural frequency ω_n, its damping factor ζ_n and the lock-in range $\Delta\omega_L$ are given by:

$$\omega_n = \sqrt{\frac{K_{VCO}K_{pd}}{NC_1}} = \sqrt{\frac{I_{ch}\Delta\omega}{\Delta V_{ctl} 2\pi NC_1}} \tag{6.42}$$

$$\zeta_n = \frac{1}{2}\omega_n RC_1 \tag{6.43}$$

$$\Delta\omega_L = 4\pi \cdot \zeta_n \cdot \omega_n \tag{6.44}$$

For the design of low frequency (kHz) operation, K_{vco}=56.5 kHz/V, K_{pd}=2.76×10^{-9} Amp/rad, I_{ch}=17.6 nA, C_1=25 pF. Based on the actual value of N, the natural frequency of our relaxation and ring oscillator PLLs will vary between 0.65 – 2.5 kHz, while the damping factor is expected to lie between 0.4-1.6. This yields a lock-in frequency of 5-20 times the natural frequency, which provides sufficient protection against jitter present on the reference input.

Figure 6.7 reveals the low frequency relaxation PLL start-up behavior for N=3 obtained from physical chip measurements. The top trace represents the supply voltage changing from 0 to 3 V while the bottom trace depicts the output voltage. The PLL converges to within 1% of

the final value (24.576 kHz) in 1.7 ms. Figure 6.8 illustrates the settling behavior while the output switches from 16.384 kHz to 32.768 kHz. In this case, the 1% settling time is approximately 1.6 ms.

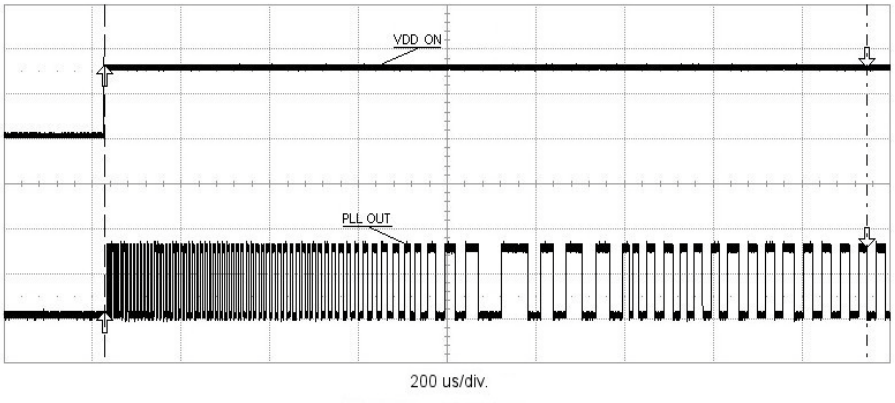


Figure 6.7. Recorded turn-on behavior of low speed relaxation oscillator PLL for N=3, i.e., f_{out}=24.576kHz.

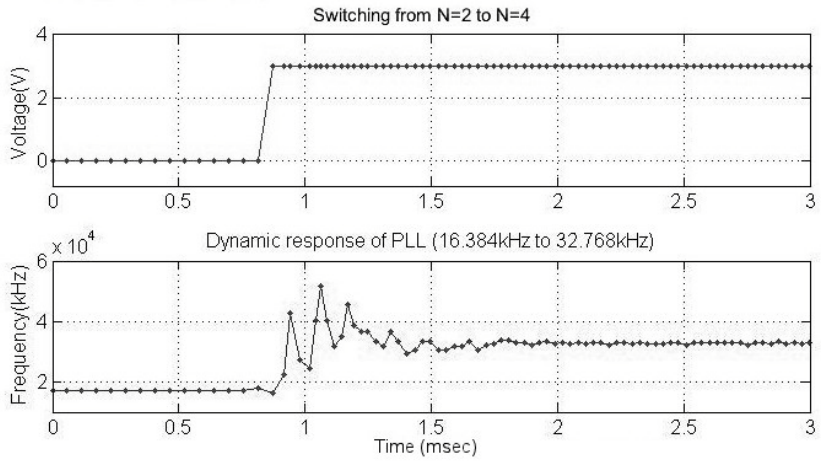


Figure 6.8. Dynamic response of low speed relaxation oscillator PLL to a frequency change from 16.384kHz to 32.768kHz.

In our design, the control voltage is inversely proportional to the output frequency, so the PLL control voltage in Figure 6.9 displays the same

settling behavior as the PLL output with different damping factors and natural frequencies.

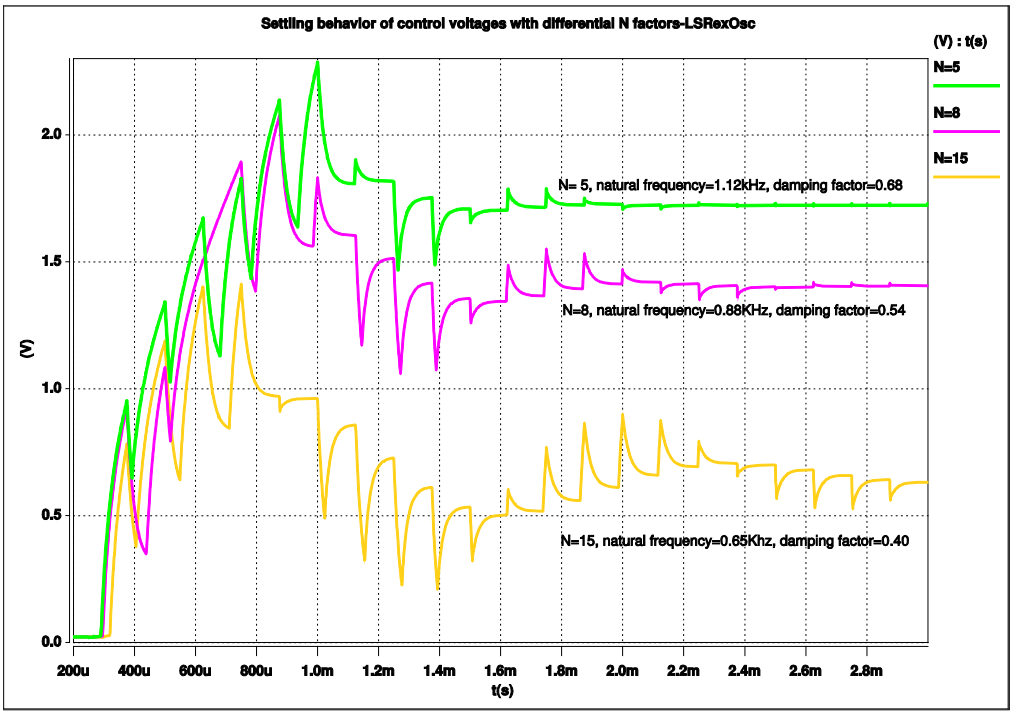


Figure 6.9. Settling behavior of control voltages while low frequency relaxation oscillator has different output frequencies.

Figure 6.10 reveals the low speed differential ring oscillator PLL start-up behavior for N=3 obtained from an extracted layout simulation. The top trace represents the supply voltage changing from 0 to 3 V while the bottom trace depicts the output voltage. The PLL converges to within 1% of the final value (24 kHz) in 2.3 ms. When power supply is 0 V, PLL output has a random status which is either 0 or 3 V.

Figure 6.11 illustrates the settling behavior while the output switches

from 40 kHz to 56 kHz. For the differential ring oscillator PLL, the 1% settling time is approximately 4.5 ms. The PLL control voltage in Figure 6.12 illustrates the settling behavior of the differential PLL output with different damping factors and natural frequencies.

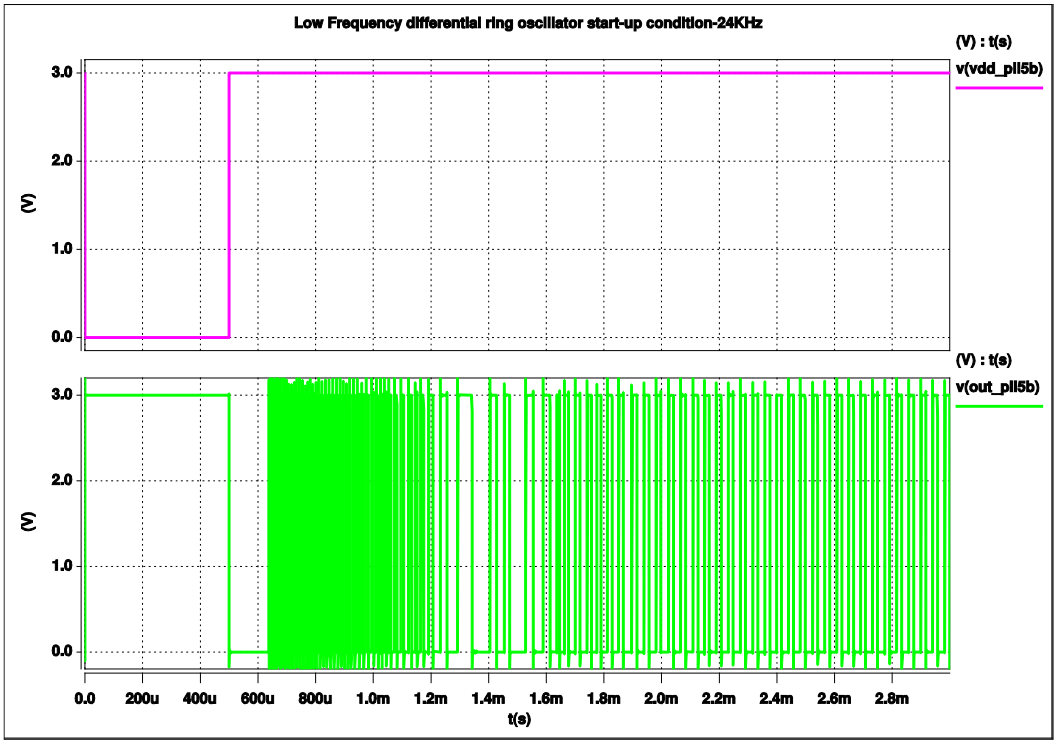


Figure 6.10. Recorded turn-on behavior of low speed differential ring oscillator PLL for N=3, i.e., f_{out}=24kHz.

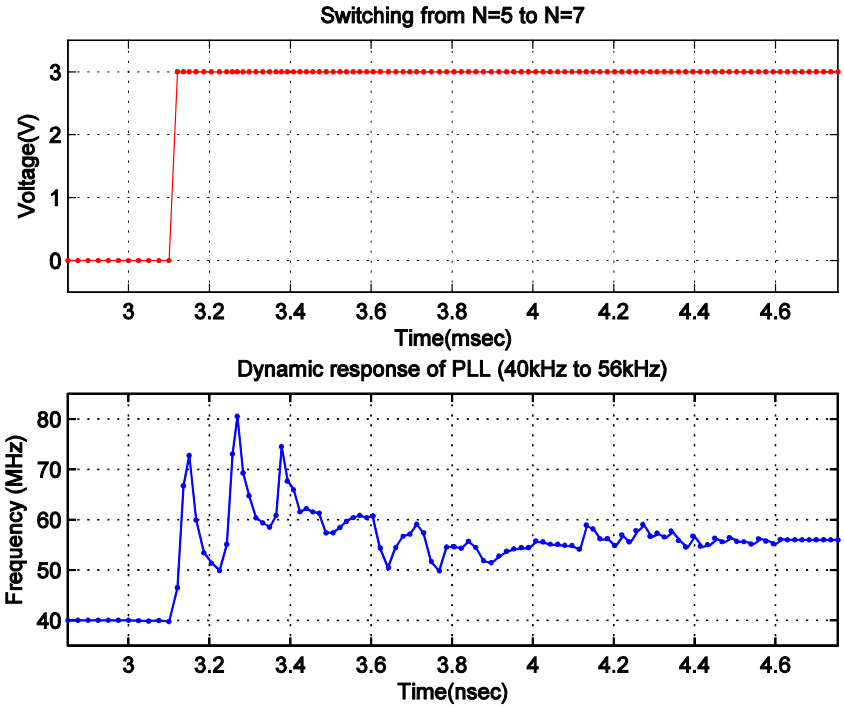


Figure 6.11. Dynamic response of low speed differential ring oscillator PLL to a frequency change from 40 kHz to 56 kHz.

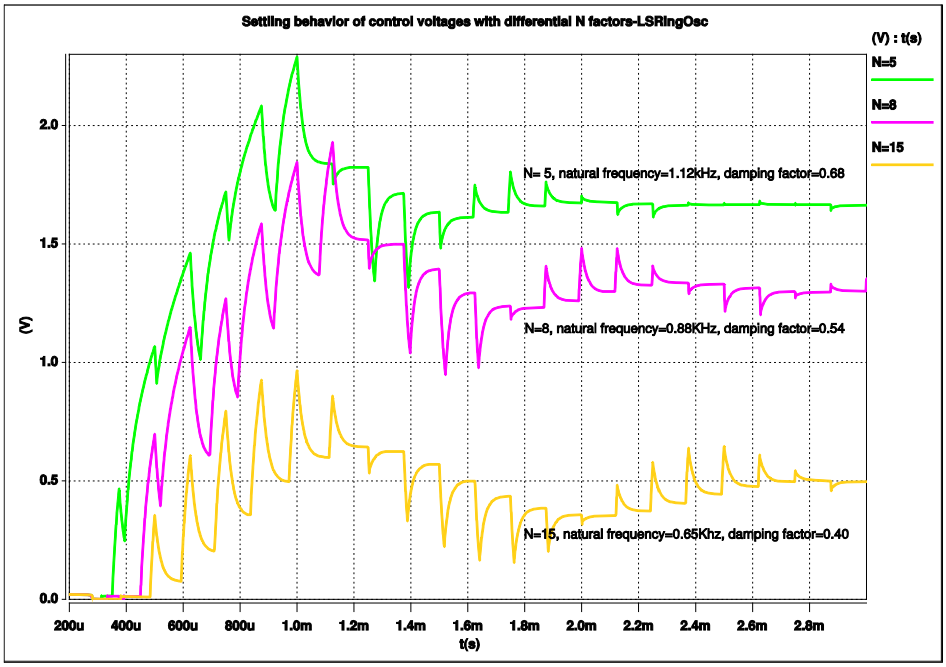


Figure 6.12. Settling behavior of control voltage while low frequency differential ring oscillator has different output frequencies.

Based on the actual value of N, the natural frequency of our high speed ring oscillator PLL varies between 1.8 – 4.3 MHz, while the damping factor is expected to lie between 0.44-1.04. Figure 6.13 reveals the high frequency ring oscillator PLL start-up behavior for N=3 obtained from an extracted layout simulations. The top trace represents the supply voltage changing from 0 to 3 V while the bottom trace depicts the output voltage. The PLL converges to within 1% of the final value (24 MHz) in 1.8 μs. Figure 6.14 illustrates the settling behavior while the output switches from 24 MHz to 40 MHz. In this case, the 1% settling time is approximately 3.9 μs. Figure 6.15 depicts the settling behavior of the control voltage when the PLL is operating under different frequencies.

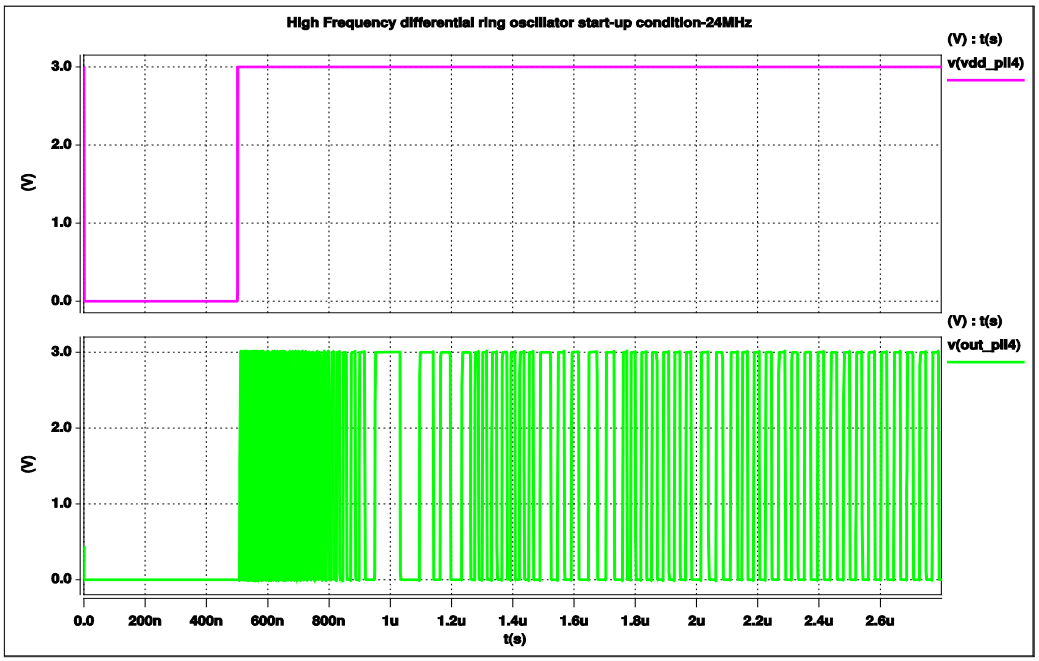


Figure 6.13. Recorded turn-on behavior of high speed differential ring oscillator PLL for N=3, i.e., f_{out}=24 MHz.

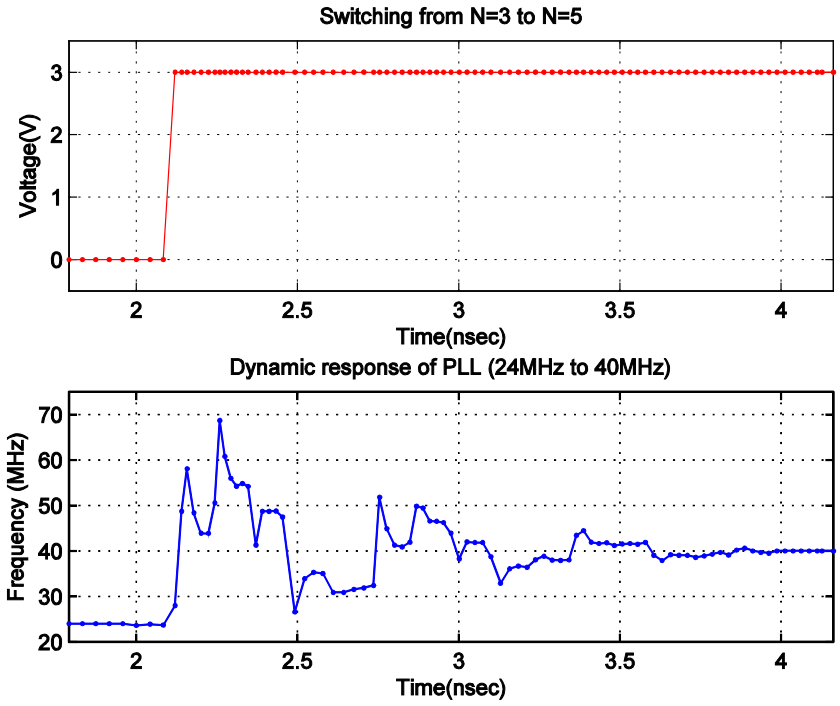


Figure 6.14. Dynamic response of high speed differential ring oscillator PLL to a frequency change from 24 MHz to 40 MHz.

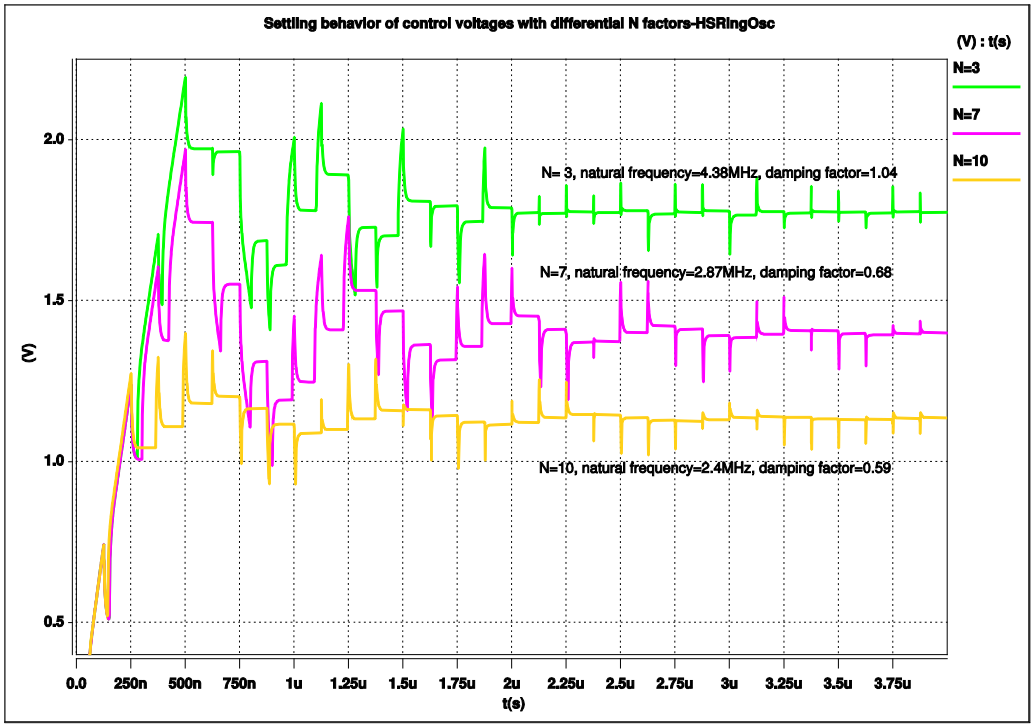


Figure 6.15. Damping factor with different N in high speed differential ring oscillator

Reference:

[1] Chapter 2 of Phase-Locked Loops, 3rd Ed., R. Best, McGraw-Hill, 1997.

[2] Chapter 2 & 5 of Phaselock Techniques, F. Gardner, John Wiley & Sons, 2005.

[3] Jimmin Chang, A. A. Abidi, and C. R. Viswanathan, "Flicker noise in CMOS transistors from sub-threshold to strong inversion at various temperatures," *IEEE Trans. on Electron Devices*, 41(11):1965-1971, November 1994.

Chapter 7

Simulation and physical testing results

In this chapter, we will present simulation and PCB testing board design and physical testing results. All circuit simulations have been performed on a layout extracted netlist and carried out by HSpice using the latest Bsim3v3.1 model parameters of the available 0.5 um CMOS process. All circuit layouts have been accomplished by MAGIC (VLSI layout tool). We have assumed a square wave reference input voltage of 8.192 kHz with 3 V swing. The physical testing results contain power dissipation and jitter measurement.

7.1 Simulation and physical testing of PLL with low speed relaxation oscillator.

To demonstrate the proper functionality of the proposed low speed relaxation oscillator PLL, we have realized the physical layout of the entire PLL. Figure 7.3 and Figure 7.4 display pictures of the final MAGIC layout and micrograph of the physical chip, respectively.

As can be seen, the VCO and the programmable digital frequency divider rather pale in comparison to the filter capacitor C_1, which fills about 60% of the entire PLL footprint. The size of the entire die is about 0.048mm^2 and the filter capacitor C_1 occupies 0.03mm^2 . To provide some extra protection against ground noise injection, the analog portion of the PLL has been protected by a guard ring.

Figure 7.1 shows the charge pump circuit. The capacitor C_2 is realized by the bottom plate parasitic of C_1 and amounts to approximately 10% of the filter capacitor. C_1 has been selected as 25 pF and C_2 is approximately 2.5 pF to provide a good settling behavior. The capacitor C_g in Figure 7.3 is used to generate a ramp and has been chosen as 0.2 pF for the10 – 150 kHz range. C_1 is the large purple area marked with C_{lcp} on the PLL layout. C_g is the yellow box with red boundary on the very left hand side of VCO block.

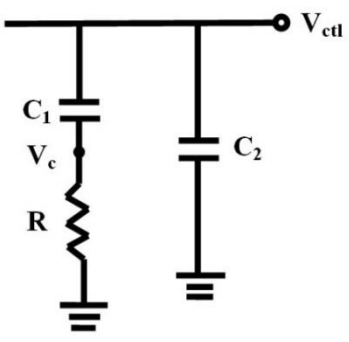


Figure 7.1. Circuit of charge pump.

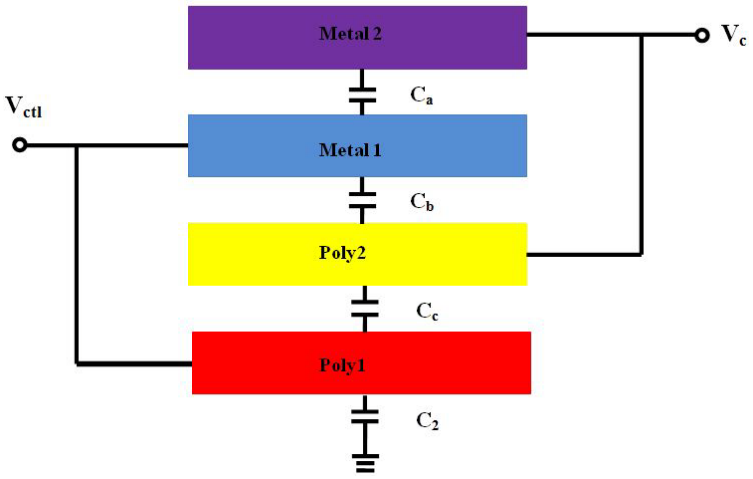


Figure 7.2. 4-layer capacitor design.

Figure 7.2 shows that C_1 actually consists of 4 layers. They are metal2, metal1, poly2 and poly1. Metal 2 and poly2 are connected to node V_c while metal1 and poly1 are connected to node V_{ctl}. The benefit of using a 4-layer instead of the traditional 2-layer design is a larger capacitance within the same area. For example, if C_1 is a poly1-poly2 capacitor, the capacitance is C_c . However, the 4-layer architecture increases the capacitance to C_a+C_b+C_c. The capacitance depends on the dielectric between the two plates and capacitance per area (μm^2) is listed in Table 7.1. As can be seen, the poly1-poly2 capacitance is dominant.

Table7.1 Capacitance per area

metal1 to metal 2	32 af/μm^2
metal1 to poly2	51 af/μm^2
poly2 to poly1	909 af/μm^2

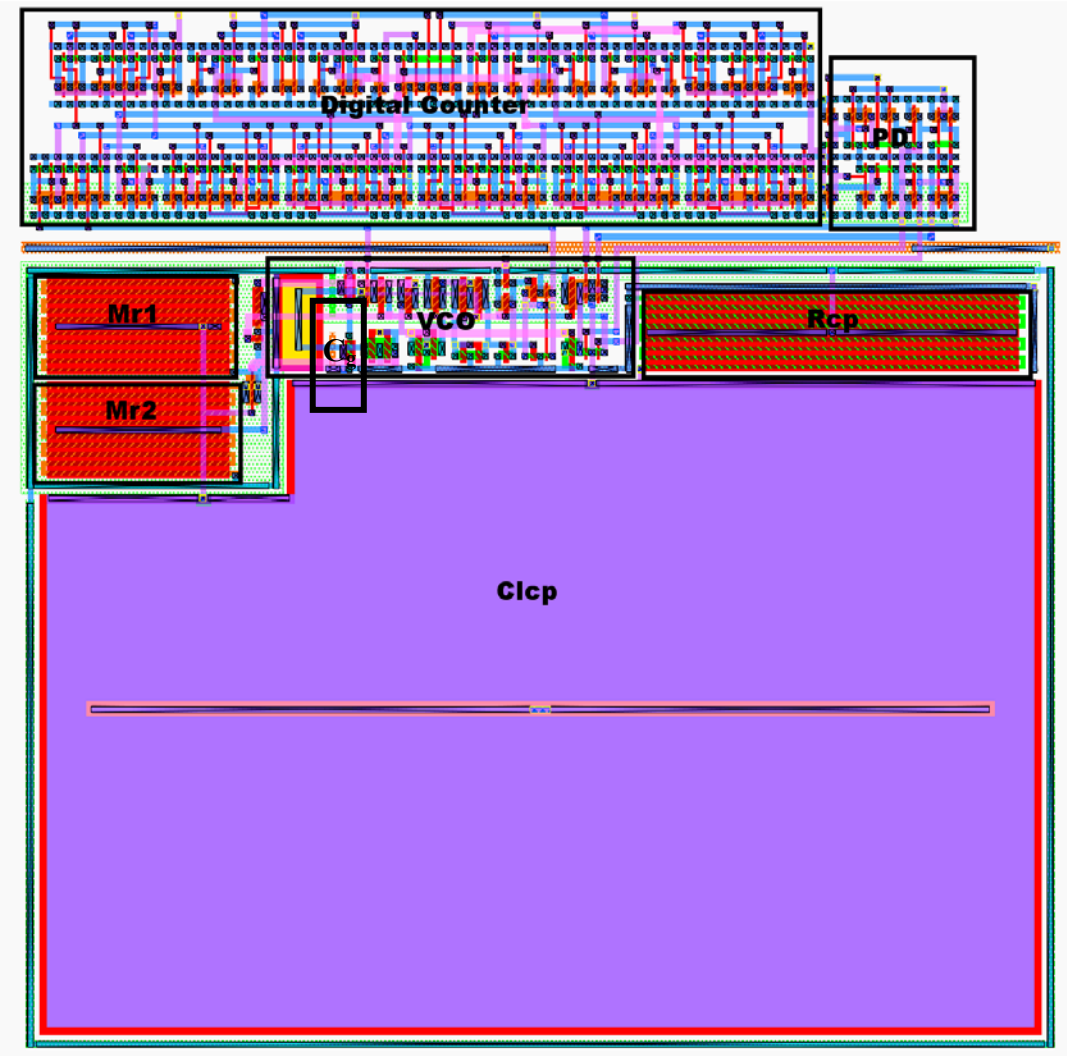


Figure 7.3. Layout of PLL with low speed relaxation oscillator (Size: 0.21 mm x 0.23 mm).

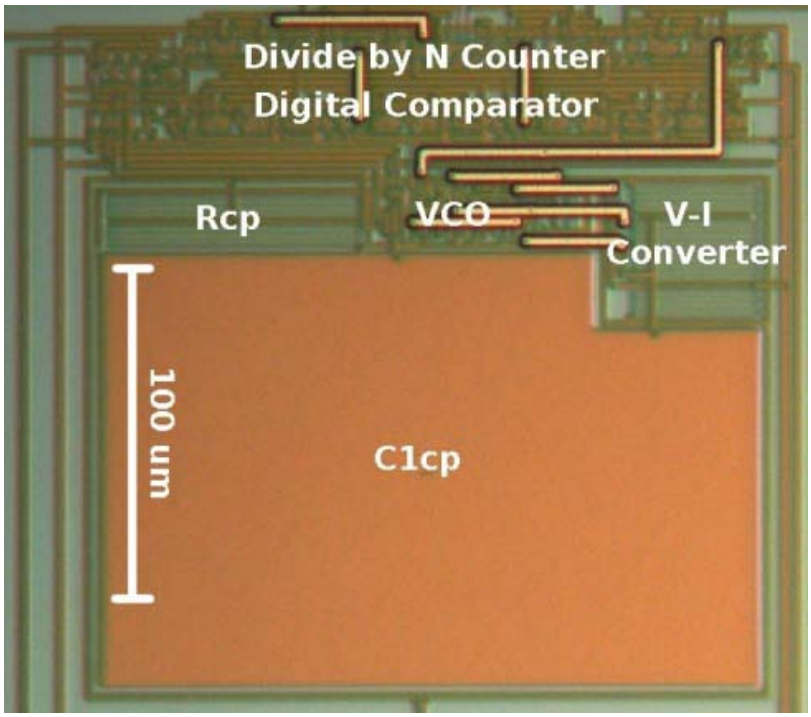


Figure 7.4 Micrograph of PLL with low speed relaxation oscillator.

Figure 7.5 reveals the dynamic response of the PLL due to a change of the digital feedback frequency divider from N=15 to N=3 as obtained from an Hspice simulation. The three depicted traces represent the output voltage of the charge pump (V_{ctl}), the feedback signal after the voltage division (V_{fb}) and the VCO reference voltage V_{ref}. The simulation results demonstrate that the PLL is stable and locks relatively quickly while N changes from 15 to 3. As expected (cf. equation (6.33) & (6.34)), the case N=15 requires visibly more settling time than N=3 (see top trace in Figure 7.5). Figure 7.6 illustrates the measured dynamic response to a change of the feedback frequency

divider from 3 to 11. Channel one (blue trace) is the switching bit from digital zero (Gnd) to one (V_{dd}). Channel two (green trace) represents the output signal of PLL.

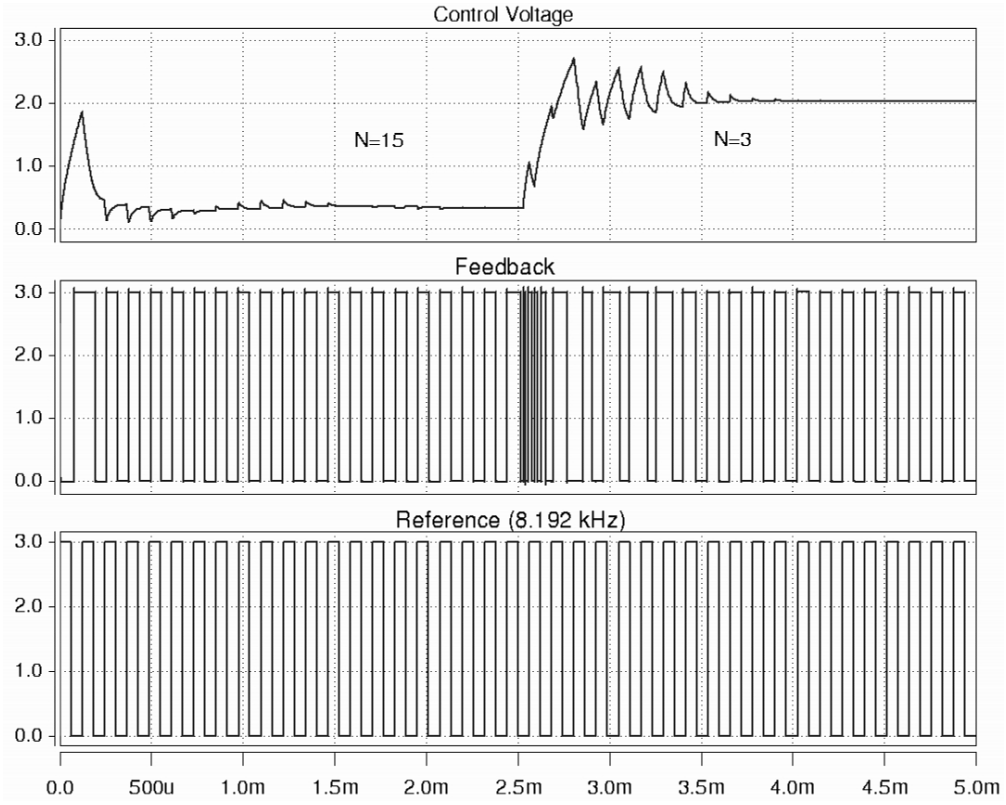


Figure 7.5. Simulated dynamic response of the proposed PLL to a change of the feedback frequency divider from 15 to 3.

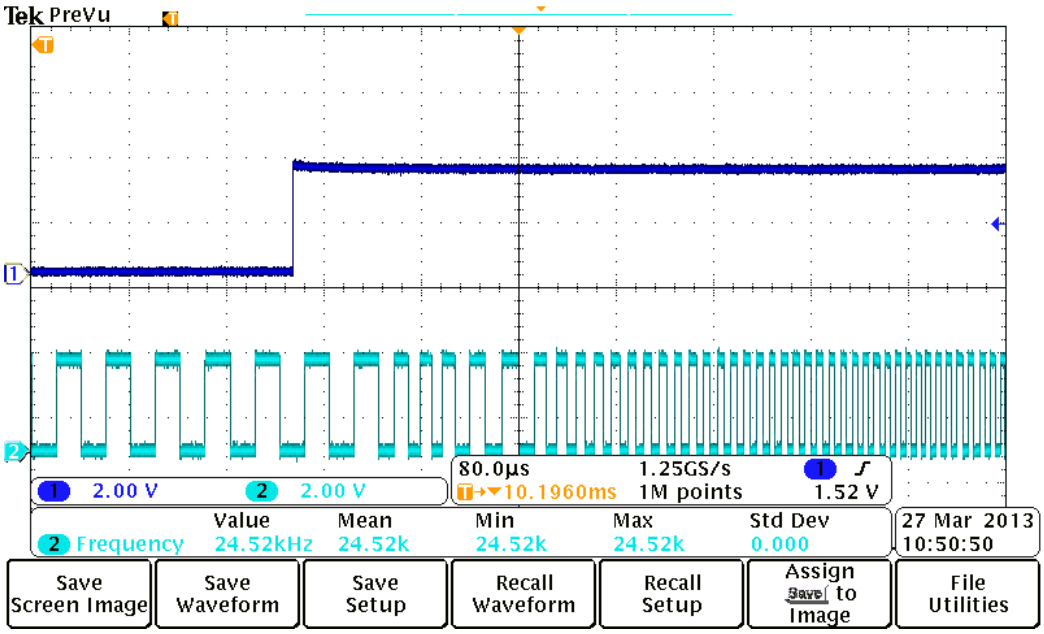


Figure 7.6. Measured dynamic response of the proposed PLL to a change of the feedback frequency divider from 3 to 11.

Simulated and measured power dissipation values of PLL are listed in Table 7.2. Note that the physical chip measurements are very close to the Hspice simulation results. The PLL is only consuming less than 2 µW power when the operating frequency is between 10-150 kHz. The values listed in Table 7.2 reveal that the power dissipation of the PLL is not strongly tied to the output frequency. In fact, the power increases by not more than 40% while the frequency quintuples from 24.576 kHz to 122.88 kHz. The measurements demonstrate that the proposed ultra low power dissipation design goal has been achieved. Since the actual phase jitter of the PLL is tightly linked to its physical operating

conditions such as substrate noise injection or cross talk between analog and digital signals, it is not possible to properly assess this parameter via simulation. However, we have obtained some indisputable numbers for this parameter from the physical implementation of the PLL in 0.5 μm CMOS technology. Table 7.2 the recorded lists phase jitter for 3 V and 3.5 V operation over the full PLL output frequency range. The relative jitter amounts to about 0.1% over the recorded range.

Table 7.3 compares the critical performance parameters of some recent low power PLL or oscillator implementations. In view of these results, we conclude that the measured PLL implementation represents an interesting alternative for very low power applications. If we were to assume that the PLL power consumption would scale linearly as the frequency, our ultra-low power PLL would consume somewhere between 2.6-5.0 mW for an output range of 25-350 MHz. These numbers would still be relatively low in comparison to other recently published work [5], [6].

Table 7.2 PLL power and jitter versus output frequency

N	F_{ref} [kHz]	F_{out} [kHz]	J_{VCO} [%]		P[μW] simulated	P [μW] measured
	3 V	3 V	3V	3.5V	3 V	3 V
3	8.192	24.576	0.11	0.11	0.91	0.90
6	8.192	49.152	0.11	0.10	1.06	1.07
9	8.192	73.728	0.11	0.10	1.21	1.30
12	8.192	98.304	0.13	0.11	1.36	1.53
15	8.192	122.88	0.14	0.12	1.51	1.76

Table7.3 Characteristics of some recent low power oscillators

References	Technol.	Supply [V]	Frequency [kHz]	Power [μW]	Area [mm^2]
This work	0.5μm	3.0	16-120	0.9-1.8*	0.04
Adnan et al [4]	0.6μm	3.3	32	20*	NA
De Vita et al [1]	0.35μm	1.0	80	1.1	NA
Lasanen et al [2]	0.35μm	1.2	200	84	0.09
Sebastiano et al [3]	65nm	1.2	100	41	0.11
Bala [5]	0.18μm	1.25	6000-24000	1120	0.14
Xintian Shi [6]	0.35μm	3.3	350000	12000*	0.09

* Complete PLL

To investigate the phase jitter in an ultra-low power PLL and compare the total jitter to our theoretical lower bound established by current noise, we recorded the phase jitter of two PLLs (PLL1 and PLL2). The VCOs of those two PLLs are slightly different as described in Chapter 5.3. PLL1 has a 2.3 V ramp voltage swing while PLL2 has a 2.85 V swing. Therefore, PLL2 is expected to have less jitter then PLL1 because of the 25% larger sawtooth swing (cf. 6.11).

The variations of the PLL output periods have been recorded with a LeCroy WaveRunner Xi-A scope. Histograms of the output period of PLL1 and PLL2 are displayed in Figure 7.7 and Figure 7.8. Evidently, the histogram closely approaches a normal distribution. We have overlaid the recorded histogram with a best-fit Gaussian distribution to compute the mean and standard deviation. The mean value stands for the long term period and the standard deviation presents the period jitter. As demonstrated in the two graphs, the jitter for PLL1 has been measured at 32.762 kHz while the jitter of PLL2 recorded at 98.304 kHz. The mean of the Gaussian distribution exactly matches the expected values of 30.518 μs and 10.172 μs, respectively.

The standard deviation of the recorded values are 30.5 ns for PLL1 and 10.2 ns for PLL2, that is almost exactly 0.1% of the mean period in either case.

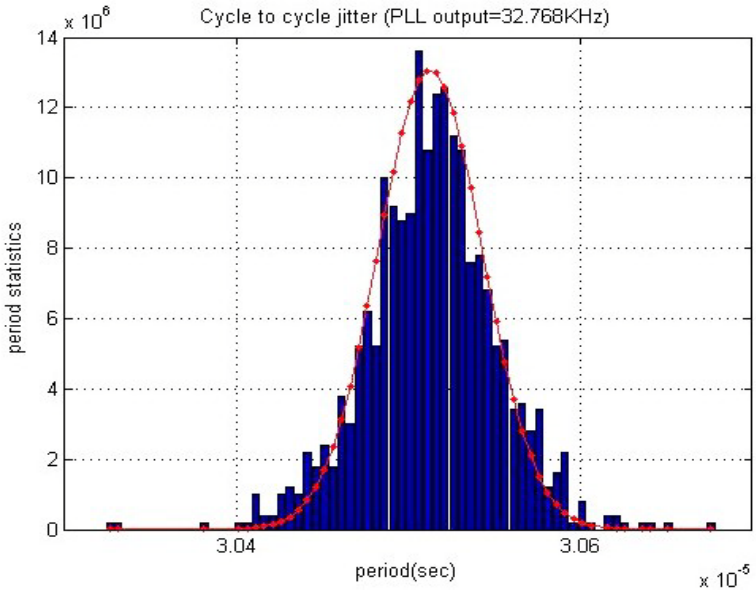


Figure 7.7. Histogram and Gaussian fit of recorded PLL1 output periods.

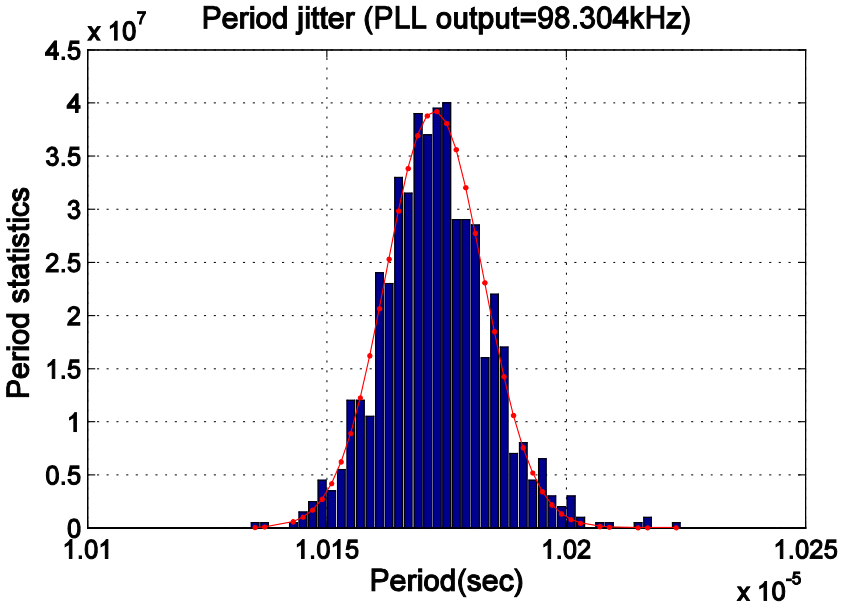


Figure 7.8. Histogram and Gaussian fit of recorded PLL2 output periods.

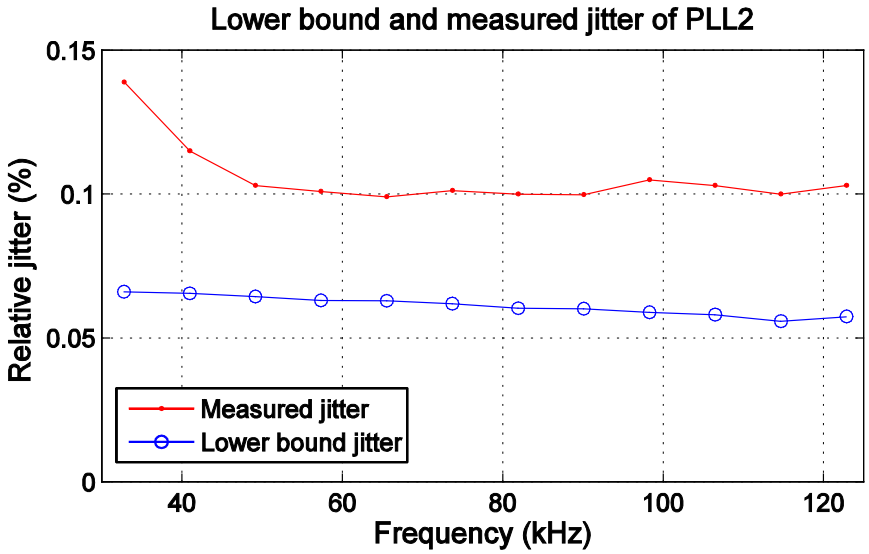


Figure 7.9. Lower bound and measured jitter of PLL2.

Both physical circuits have been operated with a 3 V supply. The recorded jitter values are summarized in Table 7.4. The numbers in Table 7.4 reveal that PLL2 yields between 3%-23% less jitter than PLL1. We attribute this improvement to the approximately 25% larger sawtooth swing, i.e., 2.3 V versus 2.85 V. Figure 7.9 compares the lower jitter bound based on J_2 in (6.11) with the actual jitter recorded for PLL2. Figure 7.10 is shown the actual LeCroy oscilloscope user interface used for jitter measurements.

Figure 7.10. LeCroy oscilloscope user interface for jitter measurement.

Table 7.4 PLL power and jitter versus frequency at 3 V

N	F_{ref} [kHz]	F_{out} [kHz]	J_{VCO} [%] PLL1	PLL2
4	8.192	32.768	0.143	0.139
6	8.192	49.152	0.113	0.103
8	8.192	65.536	0.109	0.099
10	8.192	81.920	0.104	0.100
12	8.192	98.304	0.115	0.105
14	8.192	114.69	0.123	0.100

7.2 Simulation and physical testing of PLL with low speed single-ended ring oscillator

Figure 7.11 and Figure 7.12 display pictures of the final MAGIC layout of two PLLs with different low speed single-ended ring oscillators. As shown in Figure 7.11, the resistor in the charge pump has been implemented as a passive resistor using poly2_HR with a sheet resistance of 1kΩ. The same resistor in Figure 7.12 is has been realized by a p-channel transistor placed on the left hand side of the VCO. The passive resistor requires 50 times more area than its active counterpart, however, passive resistors are linear. Based on simulation and measurements, the active resistor provides sufficient linearity for the ultra-low power design as depicted in Figure 7.14. The blue trace reflects the PLL with an active resistor and the red one is for the PLL with a passive resistor. Obviously the characteristics are very similar. Therefore, the active resistor is a better choice as far as area is concerned. Figure 7.13 shows the micrograph of the PLL with an active resistor. The die area is about 0.04 mm^2.

Figure 7.15 reveals the dynamic PLL response due to a change of the digital feedback frequency divider from N=12 to N=4 as obtained from

Hspice. The three depicted traces represent the output voltage of the charge pump (V_{ctl}), the feedback signal after the voltage division (V_{fb}) and the VCO output frequency (f_{out}). The simulation results demonstrate that the PLL is stable and locks relatively quickly while N changes from 12 to 4. Table 7.5 lists period jitter versus frequency from 24.576 kHz to 122.88 kHz for a 2.5 V and 3 V supply voltage.

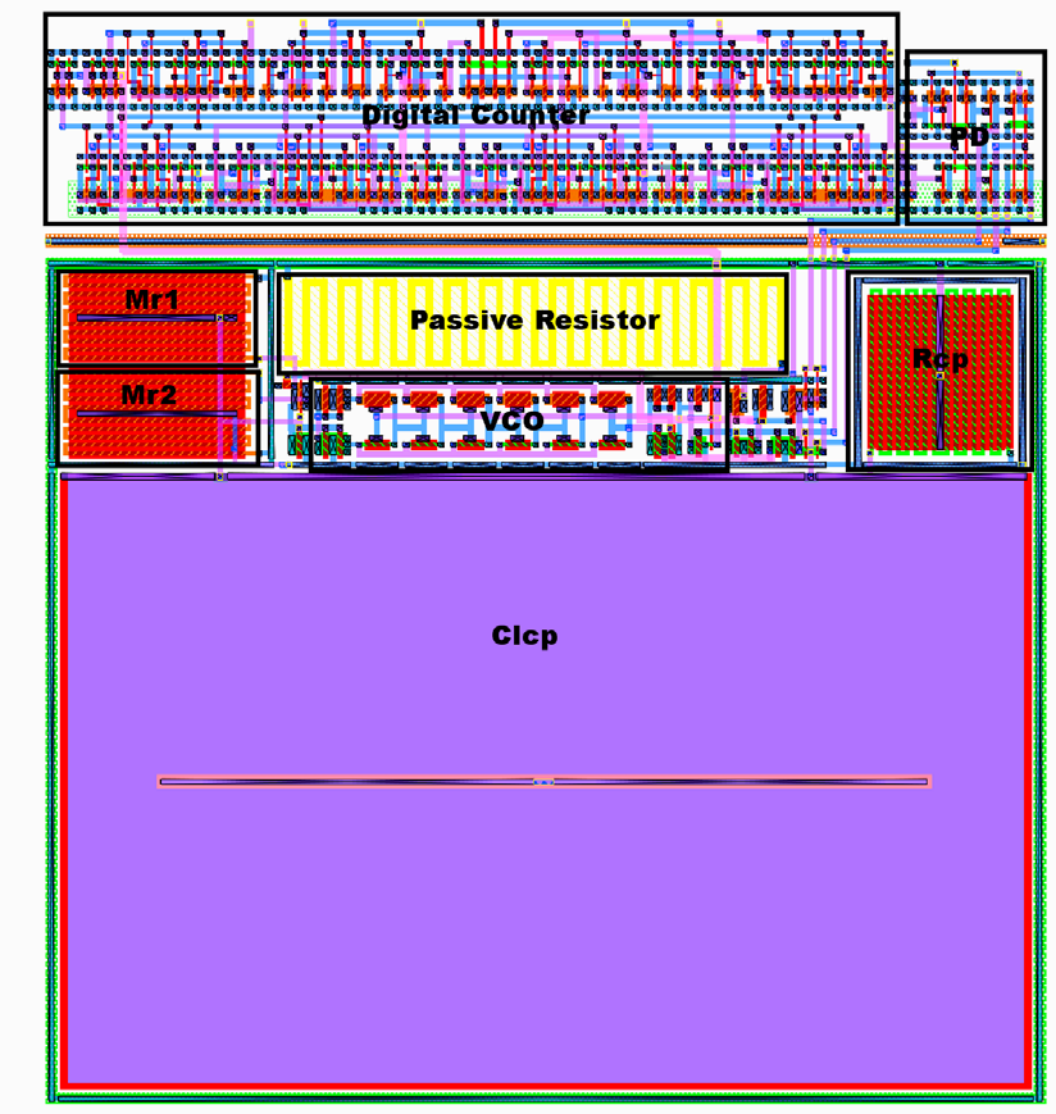


Figure 7.11. Layout of PLL with passive resistor.

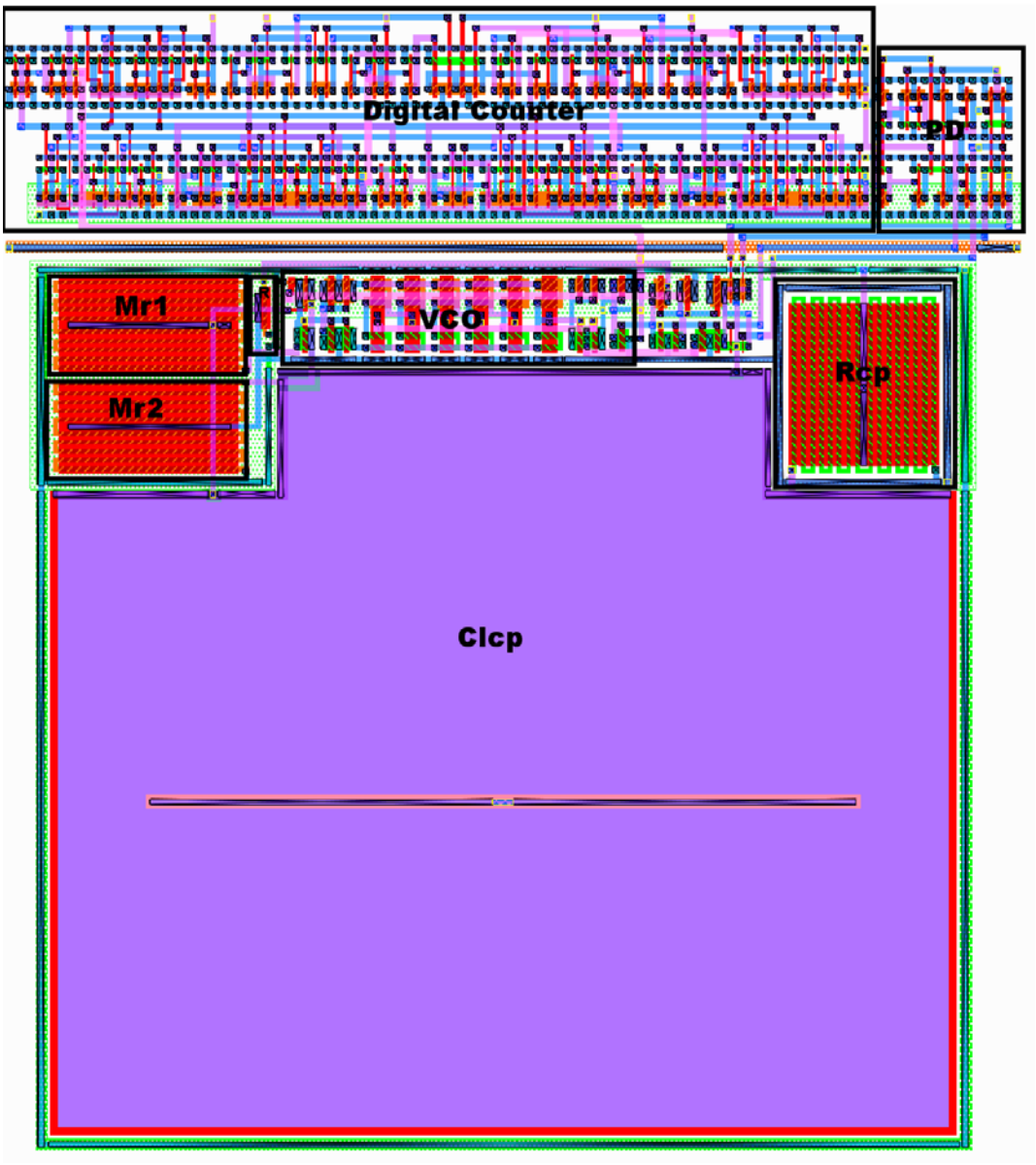


Figure 7.12. Layout of PLL with active resistor.

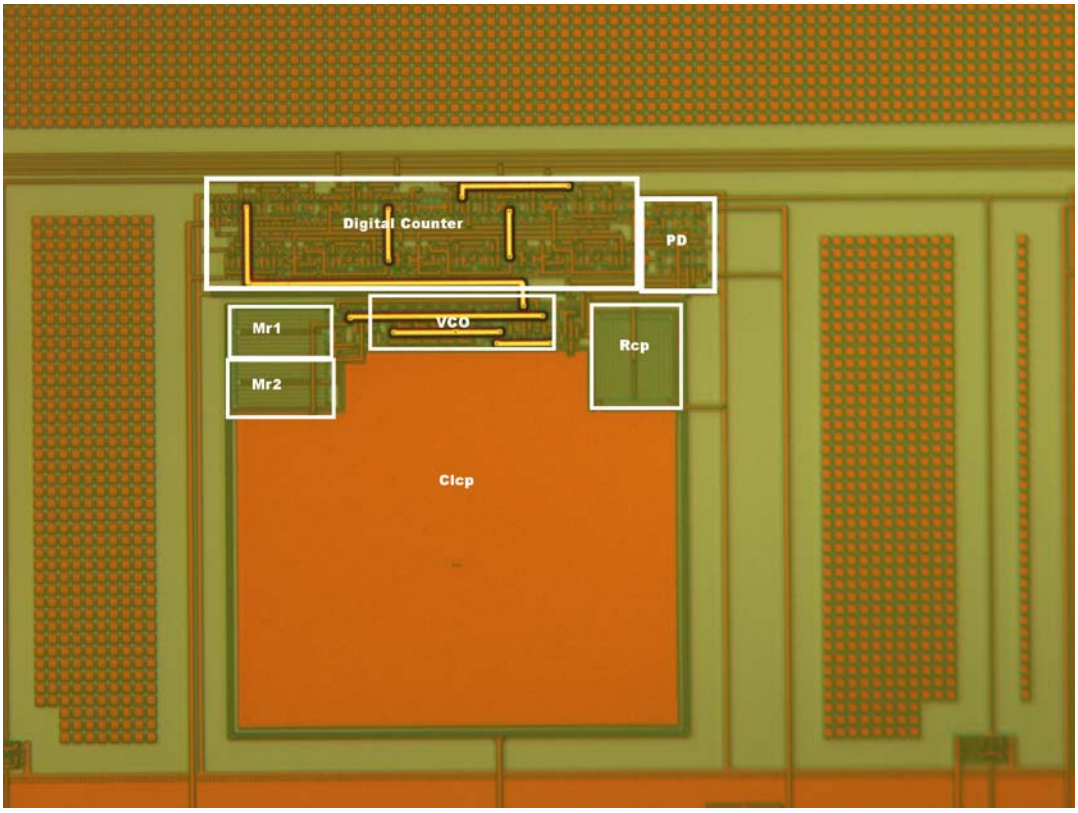


Figure 7.13. Micrograph of PLL with active resistor.

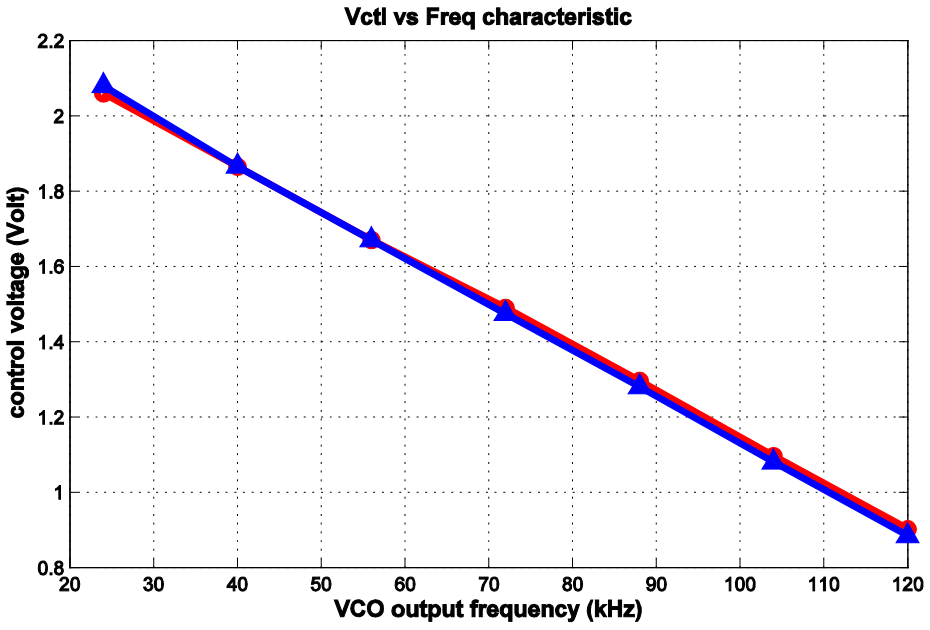


Figure 7.14 Control voltage and output frequency for both PLLs with passive and active resistor.

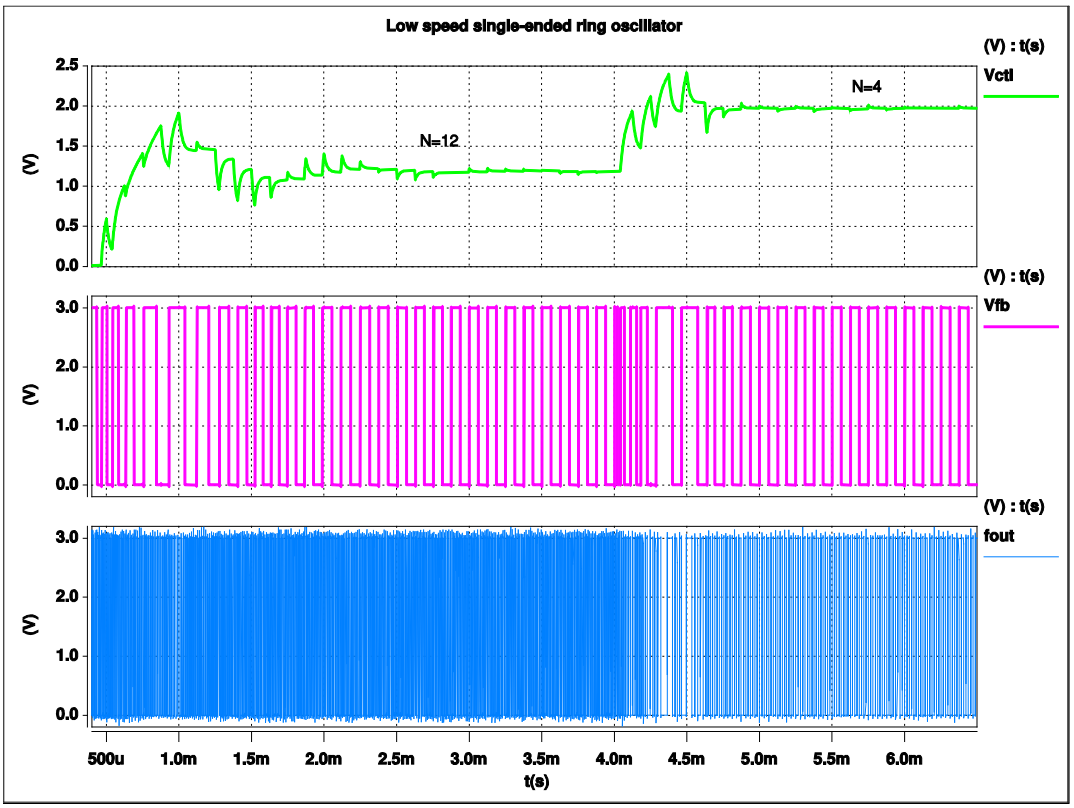


Figure 7.15 Simulated dynamic response of PLLwith single-ended ring oscillator to a change of the feedback frequency divider from 12 to 4.

Table 7.5 Phase jitter versus output frequency for PLL with single-ended ring oscillator

N	F_{ref} [kHz]	F_{out} [kHz]	J_{vco} [%]	
	3 V	3 V	2.5 V	3 V
3	8.192	24.576	0.17	0.2
4	8.192	32.768	0.14	0.14
5	8.192	40.96	0.13	0.14
6	8.192	49.152	0.14	0.13
7	8.192	57.344	0.14	0.13
8	8.192	65.536	0.12	0.13
9	8.192	73.728	0.12	0.12
10	8.192	81.92	0.12	0.12
11	8.192	90.112	0.12	0.12
12	8.192	98.304	0.12	0.11
13	8.192	106.496	0.14	0.11
14	8.192	114.88	0.11	0.11
15	8.192	122.88	0.11	0.11

7.3 Simulation of PLL with low speed differential ring oscillator

Figure 7.16 is the MAGIC layout of the PLL and Figure 7.17 represents the micrograph taken from the physical chip. Figure 7.18 reveals the dynamic response of the PLL due to a change of the digital feedback frequency divider from N=11 to N=3 as obtained from Hspice. The three depicted traces represent the output voltage of the charge pump (V_{ctl}), the feedback signal after the voltage division (V_{fb}) and the VCO output (f_{out}). The simulation results demonstrate that the PLL is stable and locks in less than 1ms, while N changes from 11 to 3. As expected (cf. equation (6.33) & (6.34)), the case N=11 requires visibly more settling time than N=3.

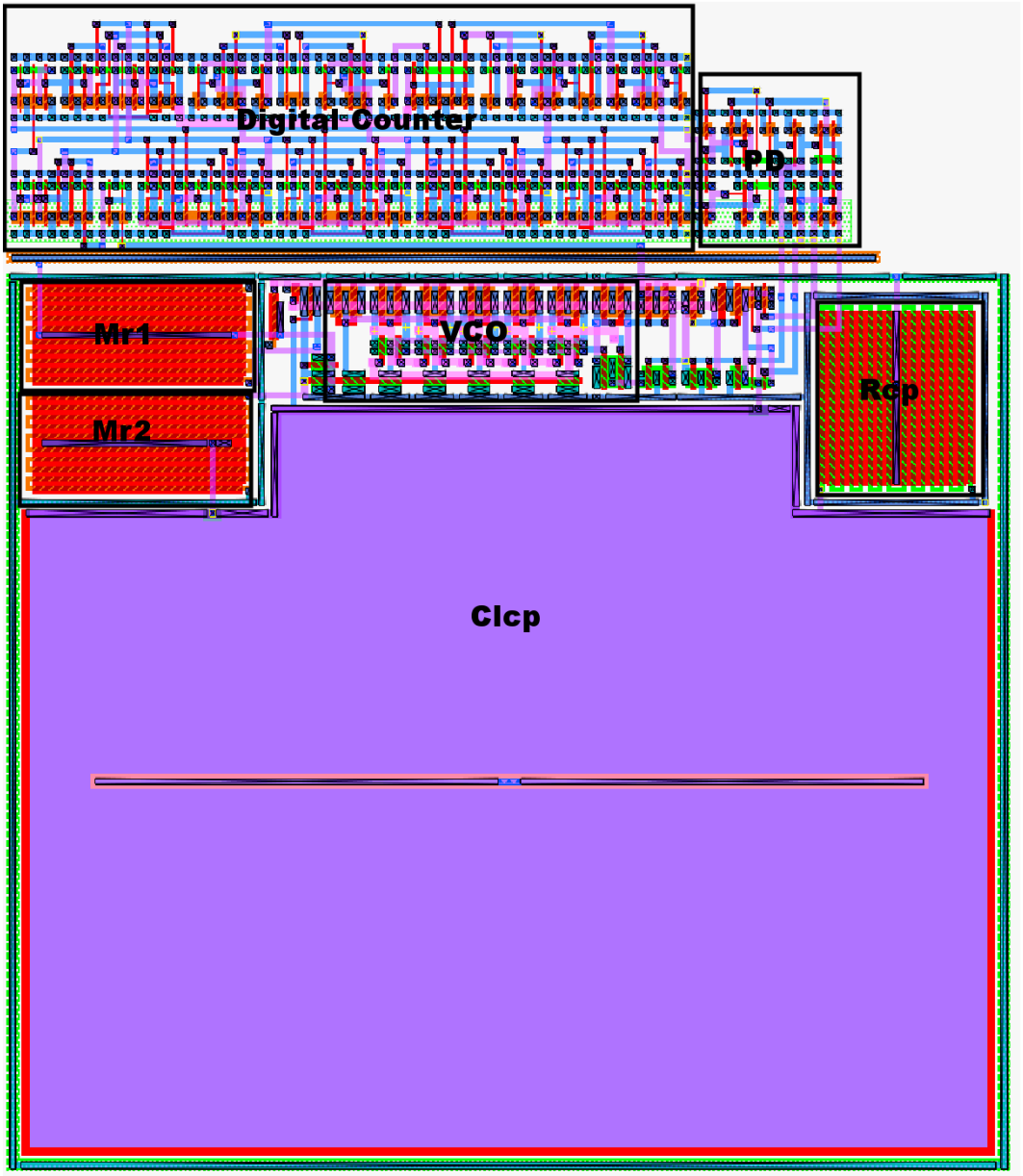


Figure 7.16 Layout of Low speed PLL with differential ring oscillator.

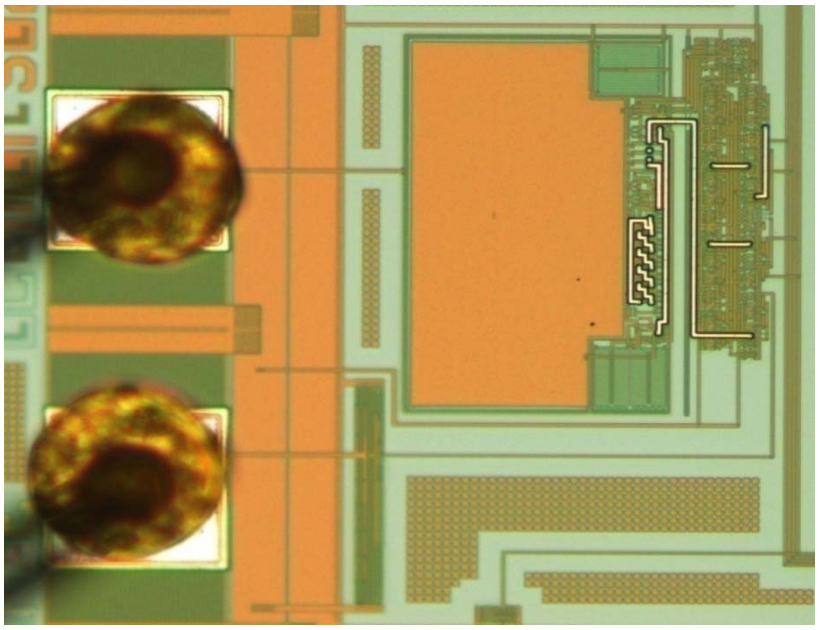


Figure 7.17 Micrograph of low speed PLL with differential ring oscillator.

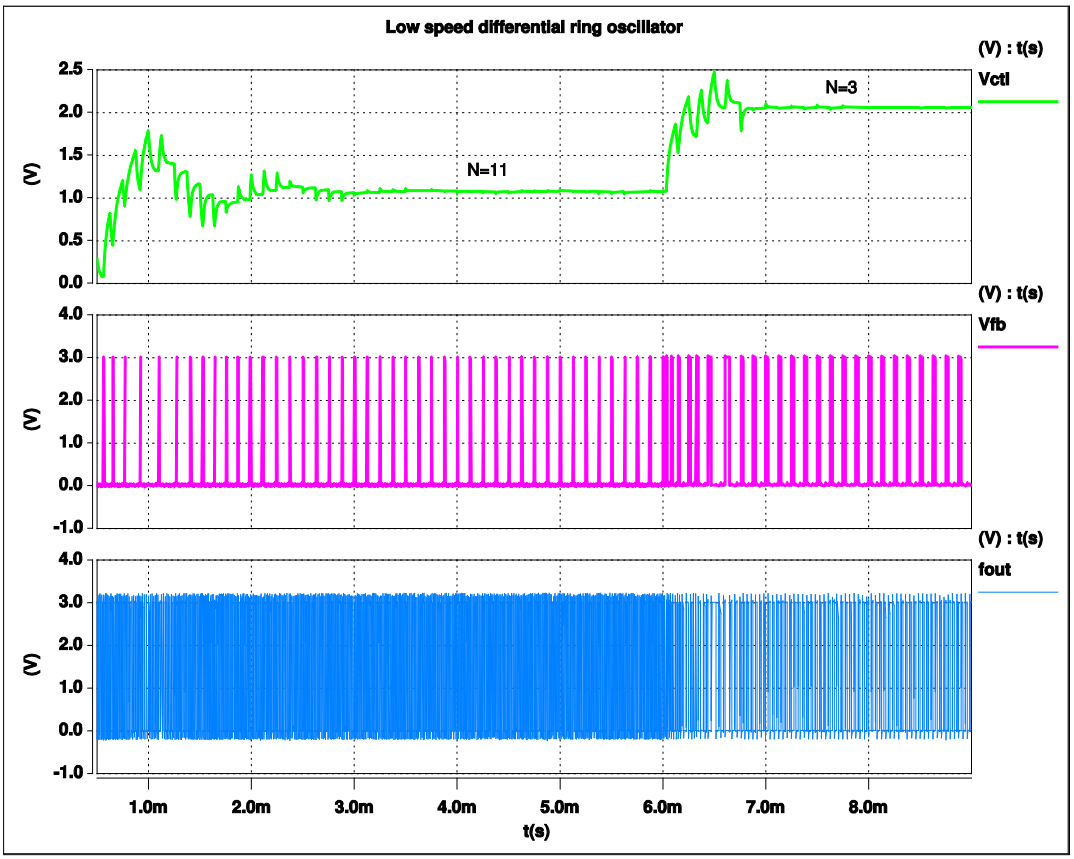


Figure 7.18. Simulated dynamic response of PLL with differential ring oscillator to a change of the feedback frequency divider from 11 to 3.

7.4 Simulation of PLL with high speed differential ring oscillator

Figure 7.19 is the MAGIC layout of the PLL and Figure 7.20 represents the micrograph taken from physical chip. Figure 7.21 reveals the dynamic response of the PLL due to a change of the digital feedback frequency divider from N=3 to N=11 as obtained from Hspice simulation. The three depicted traces represent the output voltage of the charge pump (V_{ctl}), the feedback signal after the voltage division (V_{fb}) and the VCO output (f_{out}). The simulation results demonstrate that the PLL is stable and locks relatively quickly, while N changes from 11 to 3. The RC section (charge pump) of the high speed (MHz) ring oscillator is much smaller then low speed (kHz) ring oscillator. This is obvious in Figure 7.16 and Figure 7.19.

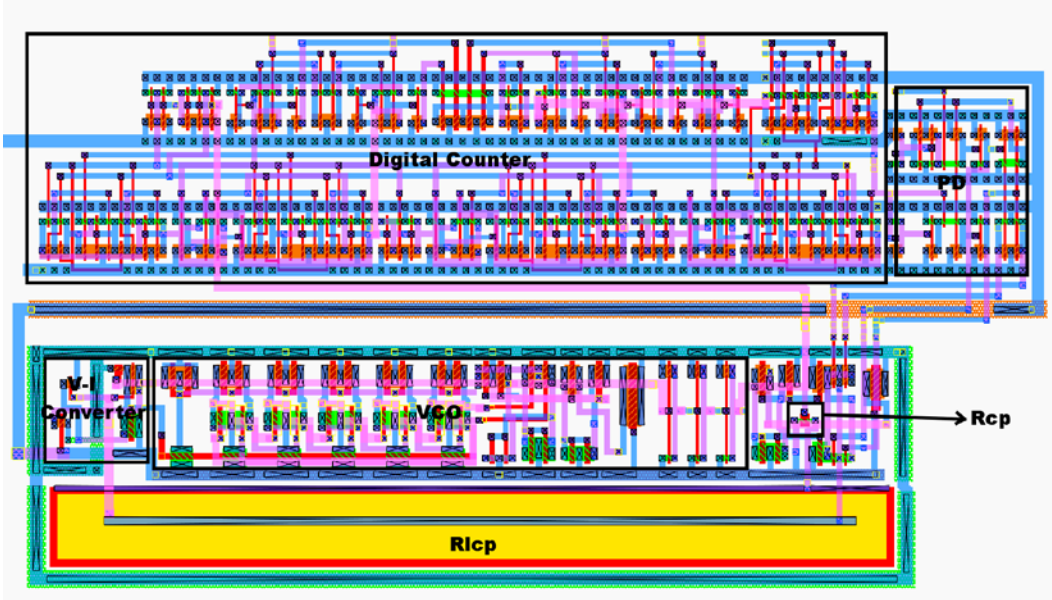


Figure 7.19 Layout of PLL with high speed differential ring oscillator

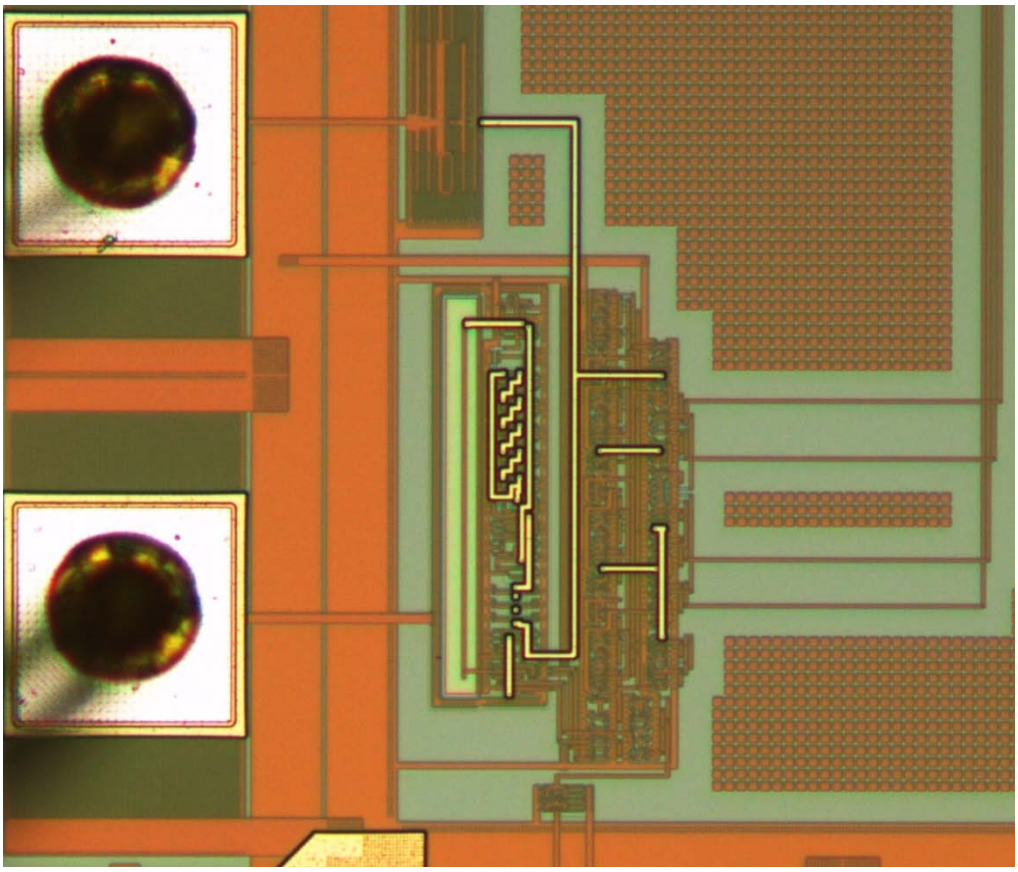


Figure 7.20 Micrograph layout of PLL with high speed differential ring oscillator

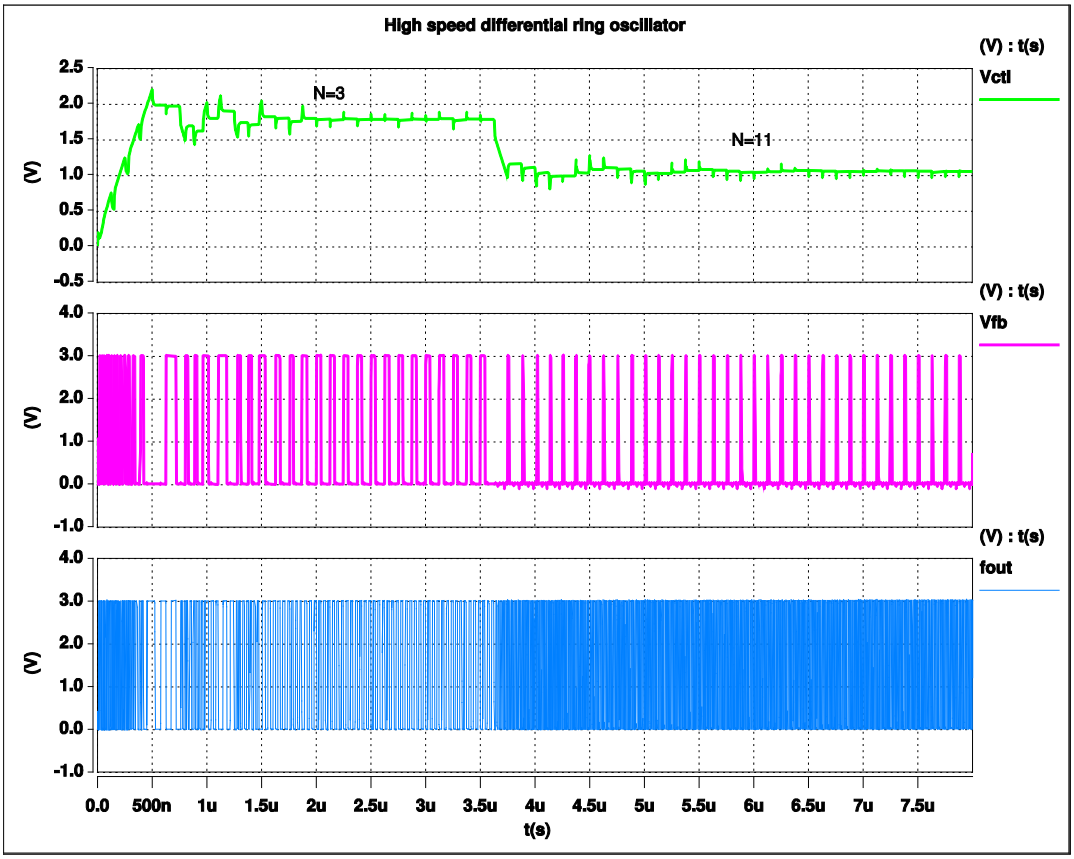


Figure 7.21. Simulated dynamic response of high speed PLL to a change of the feedback frequency divider from 3 to 11.

7.5 Testing environment set up and PCB board design

7.5.1 Test set-up

The equipment used for PLL testing includes pulse generator, power supply, high frequency oscillator and Matlab software program.

PLL testing includes two major parts. First, there is a basic functional test regarding power dissipation, settling behavior and lock-in time.

The second part involves phase jitter measurement. Normally, functional testing can be accomplished readily by a voltage meter, an amp meter and a regular scope. However, phase jitter is more difficult to measure, especially, in high speed PLL (MHz). For example, for a period jitter target of 0.1% and a PLL operating of frequency at 10 kHz , the accuracy of the digital oscilloscope has to better than 100 ns. If the operation frequency is 10 MHz , the accuracy of the scope has to be better than 100ps. The time resolution of a digital scope depends on the sampling rate of internal analog to digital converter (ADC). The smaller the phase jitter, the more precision is required. In this project, jitter of the 10 kHz range PLLs have been measured in the time domain using a Lecroy digital oscilloscope. The results have been presented in the previous sections (7.1-7.2). For high speed (MHz) PLL jitter measurements, frequency domain phase noise analysis is preferred and more realistic to be realized for university experimental conditions, because ultra high speed oscilloscopes are extremely expensive.

Figure 7.22 presents a flow diagram of low speed PLL jitter measurements. The facility Waverunner Xi-A oscilloscope from

Lecroy provides a jitter software already installed in this digital scope series. It has a functional and user friendly interface, which allows jitter measurements in real time. The results are displayed in versatile ways such as histogram and tables. However, this instrument is not able to handle jitter measurement of MHz PLLs, due to its sampling rate limitation.

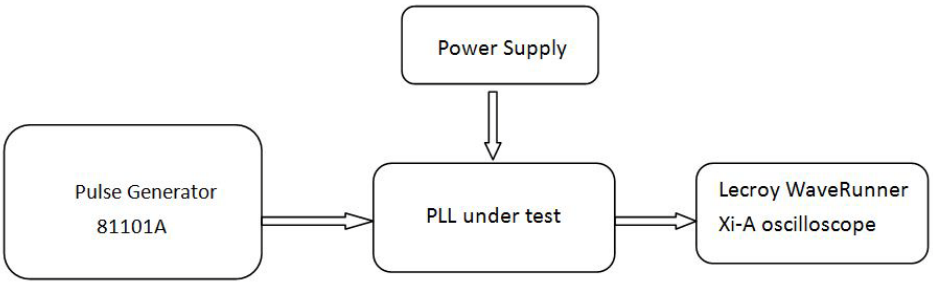


Figure 7.22. Flow diagram of low speed PLL testing setup.

Figure 7.23 illustrates the flow diagram for a high speed PLL jitter measurement. The Agilent 54855A is a GHz sampling rate oscilloscope. It is fast enough for jitter data acquisition. Matlab is used to analyze the received digital data afterwards. The fast Fourier transform (FFT) of the PLL output reveals the jitter performance in the frequency domain (cf. Chapter 3).

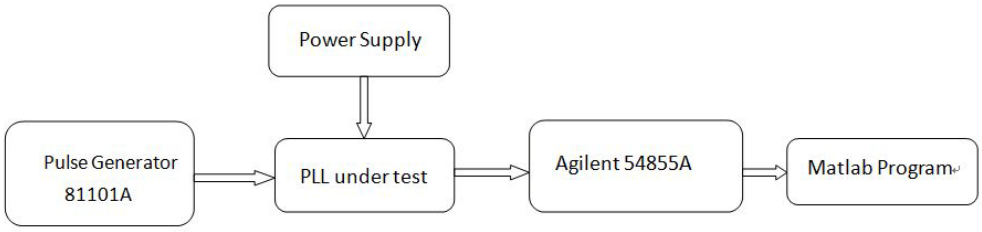


Figure 7.23. Flow diagram of high speed PLL testing setup.

The pulse generator (Agilent 81101A) we used to generate reference signals features a relative jitter of only 0.001% which is much lower than the PLL jitter, we can therefore neglect the noise induced by the reference signal. Figure 7.24 depicts a real bench test set up with all major pieces of equipments.

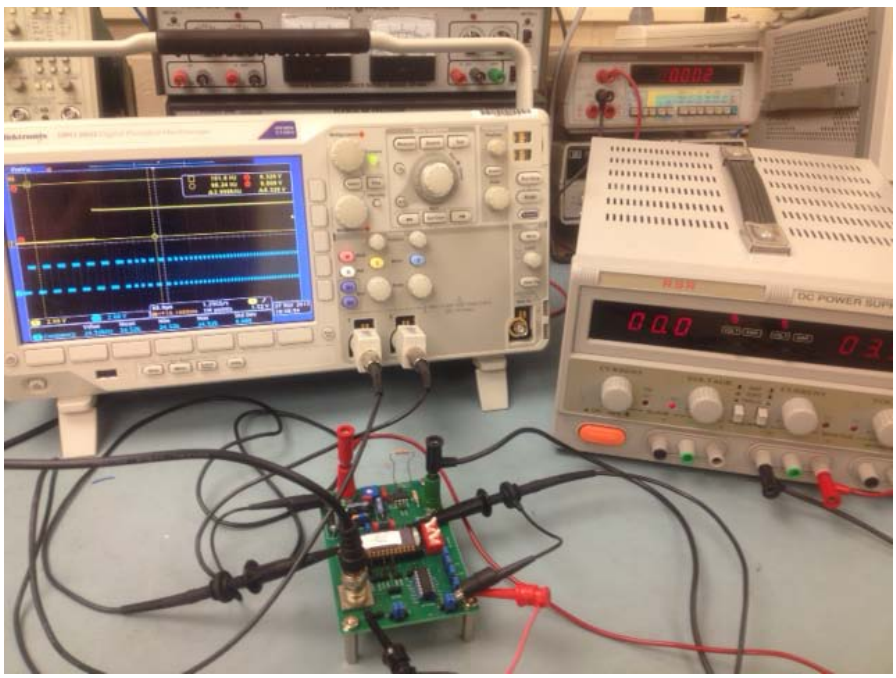


Figure 7.24. Real testing bench set up.

7.5.2 PCB design

The PCB test board has been designed in the VLSI lab at the University of Rhode Island. Figure 7.25 shows a complete chip layout with frame of one of the fabricated PLL chips.

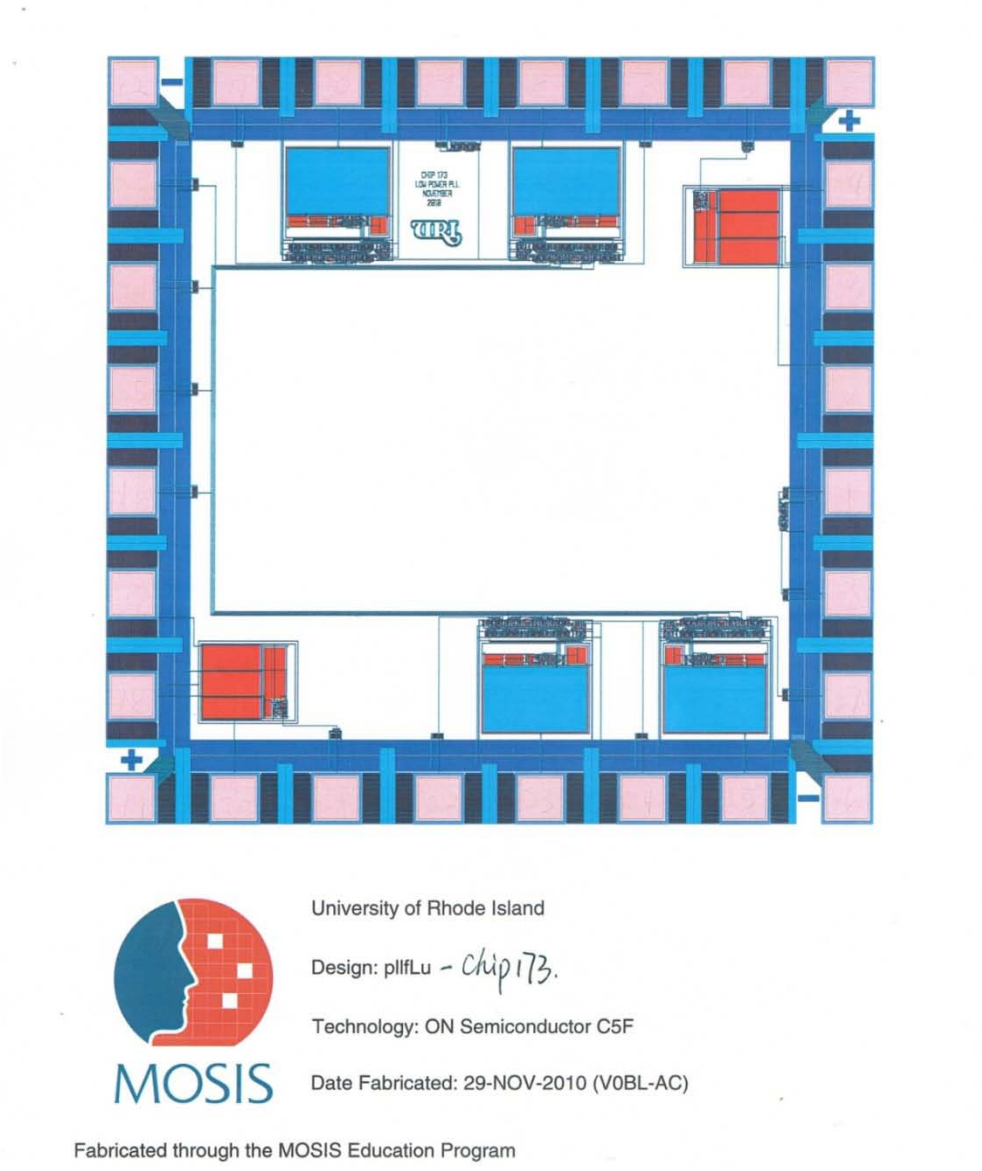


Figure 7.25 The entire chip layout with frame.

The square in Figure 7.26 represents the complete die. The unpackaged die is difficult to test and would require a probe station. For easy testing, we need to put die into a package. The solid square depicted in Figure 7.26 is the window on the package and the numbered pads around this window define the pins of the package as shown in Figure 7.28. The lines between die and pads are bonding wire.

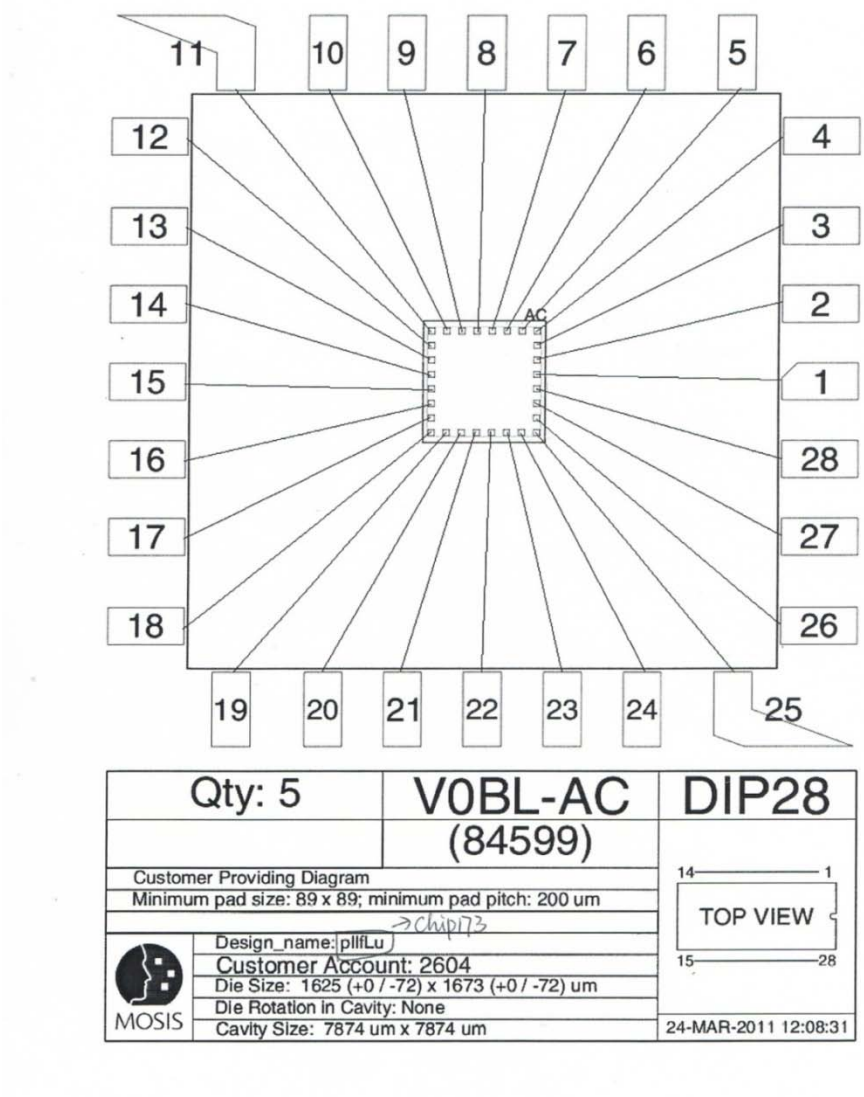
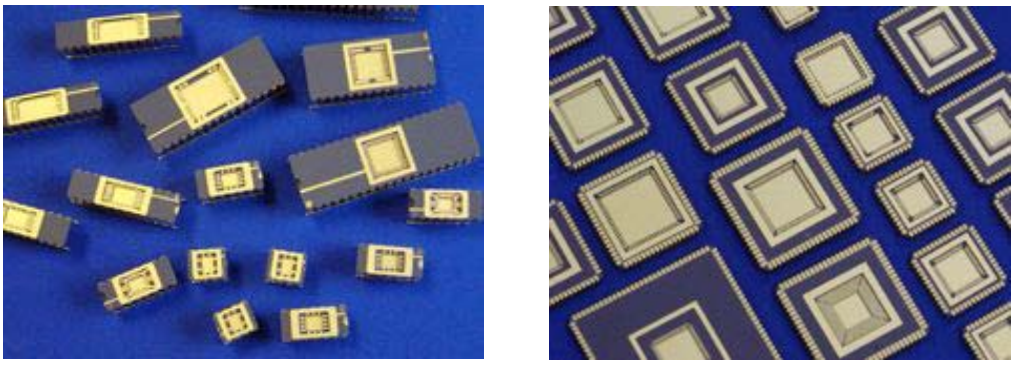


Figure 7.26. Bonding from die to standard 28 pin DIP.

If we classify packaging by way of soldering, conventional lead frame through hole and surface mount are two main categories. The package we used is the conventional lead frame standard 28 pin DIP style. The 2 package types are illustrated in Figure 7.27(a) and 7.27(b). Side braze package is a more specific name to describe the packaging style we use in our VLSI lab. Side braze packages are dual in-line packages with conventional through hole and J-bend lead configurations. They offer several advantages as listed below:

- Effective heat dissipation.
- Hermetical seal.
- Ease of PC board mounting.
- Ease of soldering and removal.
- Leads with 0.1 inch spacing.



(a) (b)

Figure 7.27. Conventional lead frame packaging (a) and surface mount packaging (b).

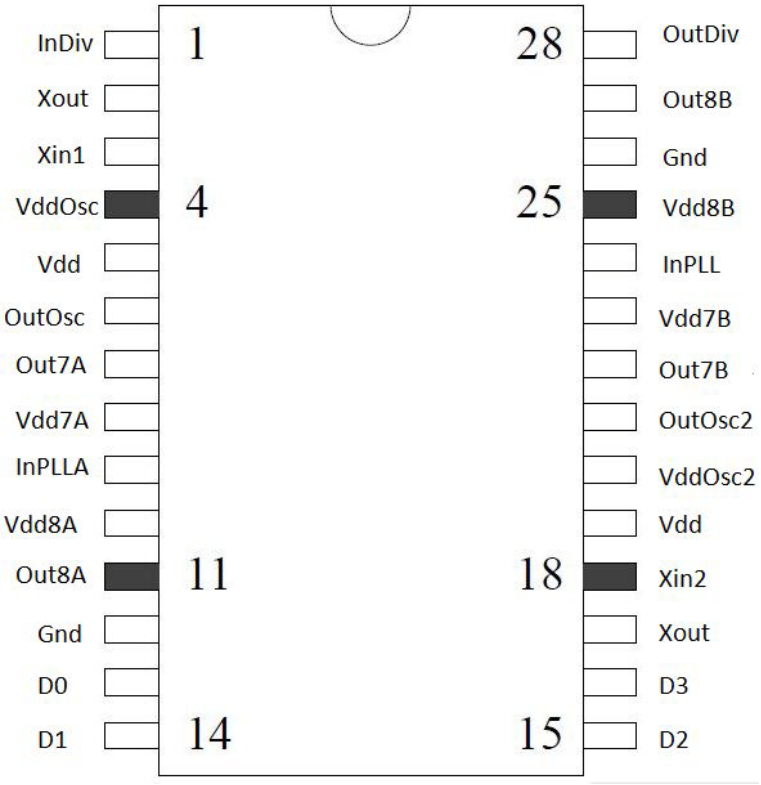


Figure 7.28. Pin diagram of chip175.

In order to minimizing the effect of power supply noise, we have utilized separate analog and digital V_{dd} pins. The supply pins on both sides of chip175, as revealed in Figure 7.28, are digital V_{dd} s and they are shorted internally. Pin V_{dd}7A, V_{dd}8A, V_{dd}7B and V_{dd}8B are analog power V_{dd} s for each PLL (4 PLLs in chip175). D0, D1, D2 and D3 are 4 common digits for all the PLLs, which control the output frequency.

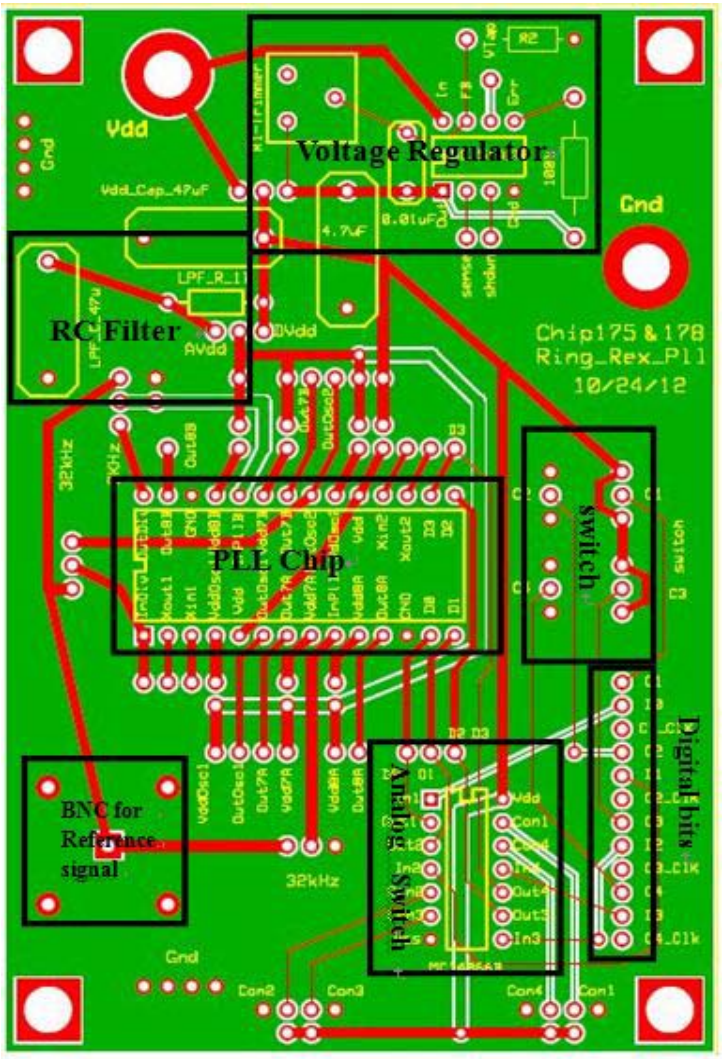


Figure 7.29. PCB board design.

Figure 7.29 shows the low speed PLL test PCB board. A voltage regulator and an RC filter are extra circuits to minimize power supply noise. The RC filter is a low pass filter with a 1kΩ resistor and 47 μF capacitor, forming a corner frequency is about 3.4 Hz.

A low power, low dropout voltage regulator (Model LP2950) from ON semiconductor has been chosen to stabilize the power supply voltage variation. The LP2950 is a micropower voltage regulators designed specifically to maintain proper regulation with an extremely low input-to-output voltage differential. This device features a very low quiescent bias current of 75 μA and is capable of supplying output currents in excess of 100mA. Internal current and thermal limiting protection is provided [7]. The low power feature is well suited for ultra low power PLL operation. An additional feature of this voltage regulator is output programmability from 1.25 V to 29 V. This wide output range provides more flexibility to obtain jitter under different supply voltages. Figure 7.30 represents a programmable regulator application set-up for a PCB.

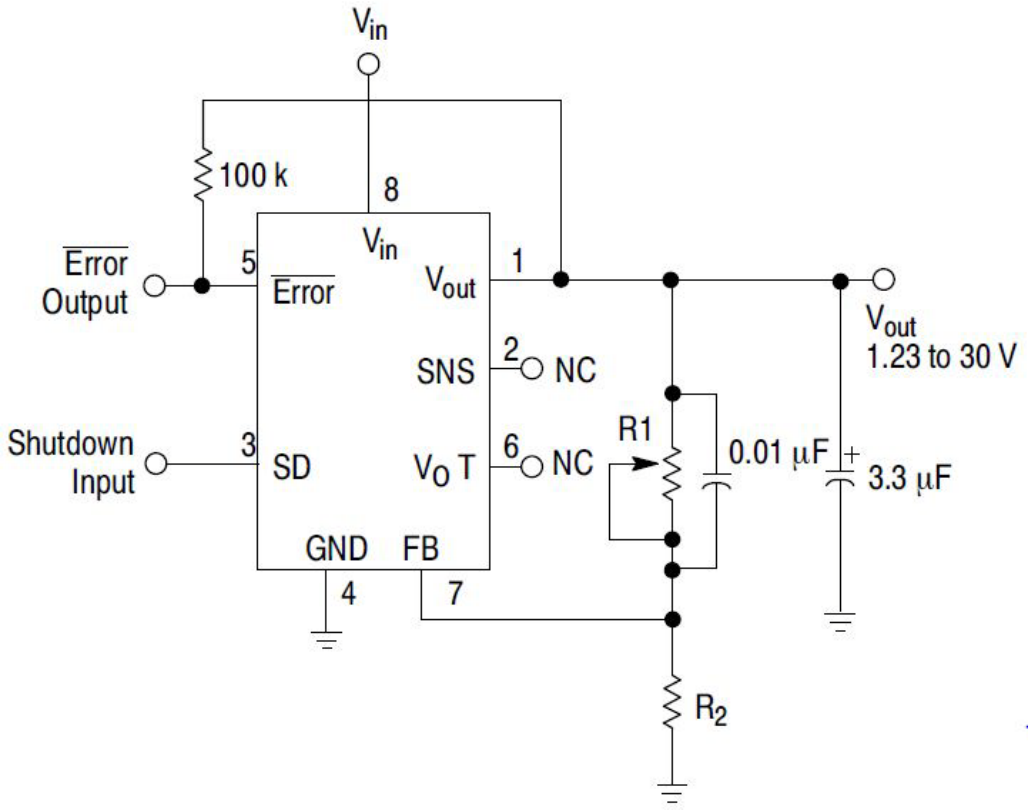


Figure 7.30. Adjustable regulator.

The complete equation for the output voltage is :

$$V_{out} = V_{ref}(1 + \mathrm{R_1/R_2}) + \mathrm{I_{FB}}R_1 \qquad (7.1)$$

Where V_{ref} is the nominal 1.235 V reference voltage and I_{FB} is the feedback pin bias current, nominally -20 nA. The minimum recommended load current of 1.0 µA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load. For better accuracy, choosing R_2 =100 kΩ reduces this error to 0.17% while increasing the resistor program current to 12 µA. In many applications

it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is one method for reducing noise. However, increasing the capacitor from 1.0 μF to 220 μF only decreased the noise from 430 μV to 160 μVrms for a 100 kHz bandwidth at 5.0 V supply. Noise can also be reduced fourfold by a bypass capacitor (C_{bypass}) across R_1. Since it reduces the high frequency gain from 4 to unity by picking C_{bypass} as 0.01 μF. When doing so, the output capacitor must be increased to 3.3 μF to maintain stability. If the application allows a 3.3 μF load capacitor, this method is effective to reduce noise. These changes reduce the output noise from 430 μV to 126 μV_{rms} for a 100 kHz bandwidth at 5.0 V supply.

A digital switch on the PCB has been used to control 4 the digital bits (D0, D1, D2, D3), which can be switched between V_{dd} (digital 1) and Gnd (digital 0). The analog switch provides high impedance for any of those 4 bits for testing purposes. The 12 pins in a column on the right hand side of the analog switch block also serve to control the 4 digital bits. Each bit is not only able to connect to either V_{dd} or Gnd, but can also be connected to with a clock signal. By doing this, the settling

behavior of the PLL can be conveniently observed on an oscilloscope.

We used a BNC cable for the reference signal to minimize the electromagnetic interference. BNCs are ideally suited for cable termination. They are used with radio, television, and other radio-frequency electronic equipment, test instruments, video signals. BNC connectors are made to match the characteristic impedance of at either 50 ohms or 75 ohms cable. They are usually applied for frequencies below 4 GHz.

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Chapter 8

Conclusions and future work

8.1 Conclusions

We have presented the designs and implementations in 0.5 μm CMOS technology of ultra-low power PLLs for the audio range based on current controlled relaxation oscillators and ring oscillators, respectively.

The relaxation oscillators generate a sawtooth output with a frequency range of approximately 20-300 kHz. P-channel transistors are employed as the comparator input pair to reduce flicker noise. Jitter resulting from random fluctuations of the two comparator input voltages is kept small by maximizing the sawtooth swing while substrate noise injection is reduced by a guard ring, which encircles all sensitive PLL components. The two current implementations realize sawtooth swings of about 80% and 93% of the supply rail, respectively, to allow investigating the dependence of the jitter on the swing.

The ring oscillators generate a trapezoidal wave with a frequency range of 10-150 kHz, which is created by the rising and falling outputs of the cascaded inverters or differential gain stages forming the oscillator. The differential gain stage has a larger common mode rejection ratio than the single-ended inverter structure. This means supply and substrate noise has less negative impact on the differential ring oscillator.

The expected reference input for all PLLs is a square wave of ¼ of the typical wrist watch crystal frequency, i.e., 8.192 kHz. A 4-bit digital comparator allows the user to pick the output as an integer multiple of the reference frequency up to a maximum of 122.88 kHz (for divide by N counter) or 131.072 (for divide by N+1 counter). Experimental results have shown that the two relaxation oscillator based PLLs settle rapidly for all values of N and operate between 8.192 kHz - 122.88 kHz with only 0.8-2 μW of dissipated power under a single 3 V supply. The measured relative jitter for both PLLs are around 0.1%.

We have derived a theoretical lower bound for the period jitter of an ultra-low power audio-range PLL based on a relaxation oscillator. The

value of the lower bound scales as the inverse of the selected ramp current I_r. The selected maximum ramp current of 70 nA yields a lower relative jitter bound of approximately 0.07%. The measured relative jitter of the PLL is between 0.11-0.14% for V_{dd}=3 V and between 0.10-0.12% for V_{dd}=3.5 V. These values are approximately 70% larger than the predicted lower bound.

We have also provided a compact expression to assess the PLL jitter. This theoretical expression can be applied to both relaxation oscillator based and ring oscillator based PLLs. The formula differentiates between jitter induced by (injected) voltage noise, device current noise and equivalent noise produced by the PD and the filter circuit. The numerical results predict that current noise induced jitter will be prominent in ultra-low power and low frequency applications. The device noise can therefore serve as a realistic lower bound for the expected jitter. The presented expression has been tested by two physical implementations. The measurements revealed that the suggested predictor accounts for approximately 50% of the actually recorded jitter. Since the predicted values diminish with frequency, they do not serve equally well to predict jitter in high-frequency

applications. A high speed (MHz) differential ring oscillator based PLL has been fabricated and we expect to obtain some measured jitter numbers to discuss the lower jitter bound theory in high speed applications and the dependence of jitter on power consumption and the number of stages.

8.2 Future work

1. Do more research about phase detector noise and charge pump noise.
2. Derive a more comprehensive expression to access jitter of an entire PLL.
3. Try to find a more realistic model for power and substrate noise.
4. Study different jitter behavior of high speed PLLs and finish the physical testing of MHz differential ring oscillator PLL.

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